



BMR510

Dual - phase integrated power stage up to 160 A peak

The BMR510 is a dual-phase integrated power stage with a continuous output current of 80A, and a peak current of 160 A.

It comes in a compact footprint of just 0.9 cm² / 0.14 in² and is available with either LGA or solder bump termination.

The device is designed with the power stages located on top for the most effective top-side conducted cooling, and delivers excellent thermal results.

The BMR510 features protection mechanisms such as over-current protection and over-temperature protection. An enable input is provided, and the module accepts tri-state PWM inputs.



Key features

- High efficiency up to 93% at light load, 87.5% at full load.
- Parallelable with other units
- Remote control
- Current and temperature reporting
- Excellent thermal performance
- 0.9 cm² / 0.14 in² compact footprint
- Halogen-free

Soldering methods

- Reflow soldering, LGA and solder bump options

Key electrical information

| Parameter | Values |
|----------------------|-----------------------|
| Input voltage range | 4.5 - 15 V |
| Output voltage range | 0.5 - 1.8 V |
| Max output current | 80 A TDC / 160 A peak |

Mechanical

10 x 9 x 7.63 mm / 0.39 x 0.35 x 0.30 in (without output capacitors)

10 x 9 x 9.5 mm / 0.39 x 0.35 x 0.37 in (with 24 output capacitors)

Application areas

- Designed for AI applications
- Used by CPU, GPUs, IPUs, high-performance ASICs

Product options

The table below describes the different product options.

| Example: | BMR510 | 1 | 04 | 1 | /002 | C | Definitions |
|---------------------------------|--------|---|----|---|------|---|--|
| Product family | BMR510 | | | | | | |
| Mounting options | | 1 | | | | | 0 = solder bump 1 = LGA |
| Product variants | | | 04 | | | | 03 = 3.3V VCC power stages 04 = 5V VCC power stages |
| Mechanical configuration | | | | 1 | | | 1 = 9.5 mm height with 24 output capacitors (528 µF) 4 = 7.63 mm height without output capacitors |
| Configuration code | | | | | /002 | | /002 = 2 phases |
| Packaging options | | | | | | C | C = Antistatic tape and reel packaging |

For more information, please refer to [Part 2 Mechanical information](#).

If you do not find the variant you are looking for, please contact us at [Flex Power Modules](#).

Order number examples

| Part number | V _{IN} | V _{OUT} | configuration |
|-----------------|-----------------|------------------|--|
| BMR5100034/002C | 4.5-15 V | 0.5–1.3V | 3.3V VCC power stages, without output capacitors, solder bump, tape and reel package |
| BMR5101041/002C | 4.5-15 V | 0.5-1.8 V | 5V VCC power stages, with 24 output capacitors, LGA, tape and reel package |

Part 1: Electrical specifications

Absolute maximum ratings

Stress in excess of the defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits*, are normally tested with one parameter at a time exceeding the limits in the electrical specification.

| Characteristics | | min | typ | max | Unit |
|--|---------------------------------------|--------------|-----|----------|------|
| Operating temperature (T _{P1}) | | -40 | | 125 | °C |
| Storage temperature | | -40 | | 125 | °C |
| Input voltage (V _{in}) | | -0.3 | | 20 | V |
| Signal I/O voltage | EN, PWM, ISEN, TSEN (BMR510X03X) | -0.3 | | VCC+0.3 | V |
| | EN, PWM ISEN, TSEN (BMR510X04X) | -0.3 -0.3 | | 6 3.6 | V |
| Driver and logic supply | VCC (BMR510X03X) | -0.3 | 3.3 | 4 | V |
| | VCC (BMR510X04X) | -0.3 | 5 | 6 | V |

Reliability

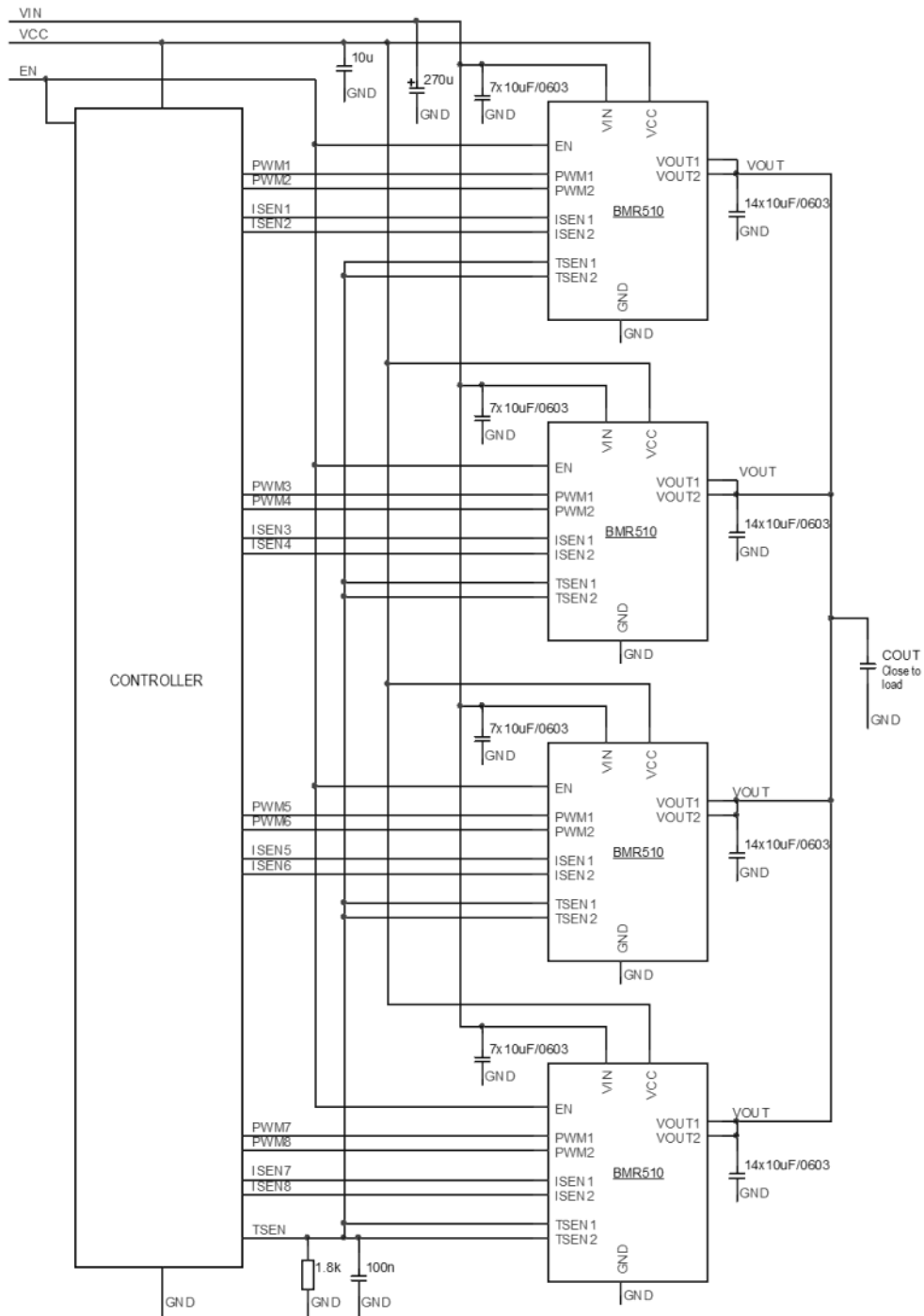
Failure rate (λ) and mean time (50%) between failures (MTBF= 1/ λ) are calculated based on *Telcordia SR-332 Issue 4: Method 1, Case 3, (80% of I_{out}, T_{P1}=40°C)*.

| BMR510XX34/002 | Mean | 90% confidence level | Unit |
|---|------|----------------------|-------------|
| Steady-state failure rate (λ) | 15 | 22 | nfailures/h |
| Standard deviation (σ) | 5.5 | | nfailures/h |
| MTBF | 65.1 | 44.66 | MHr |

| BMR510XX44/002 | Mean | 90% confidence level | Unit |
|---|-------|----------------------|-------------|
| Steady-state failure rate (λ) | 25 | 30 | nfailures/h |
| Standard deviation (σ) | 4 | | nfailures/h |
| MTBF | 40.78 | 33.79 | MHr |

| BMR510XX41/002 | Mean | 90% confidence level | Unit |
|---|-------|----------------------|-------------|
| Steady-state failure rate (λ) | 30 | 35 | nfailures/h |
| Standard deviation (σ) | 4.2 | | nfailures/h |
| MTBF | 33.81 | 28.59 | MHr |

Typical application diagram



Typical application circuit for 8 phases rail

Notes:

1. Value of output capacitance will depend on the application and load transient requirements.
2. TSEN filter values might be adjusted if connecting together TSEN of more than 16 phases.

Electrical specifications for BMR510X034/002 (VCC=3.3V, without output capacitors) — Control and Monitoring

$T_{P1} = -40\text{ °C}$ to 125 °C , $V_{in} = 12\text{ V}$, $V_{CC} = V_{EN} = 3.3\text{ V}$, unless otherwise specified under Conditions.

Typical values given at: $T_{P1} = +25\text{ °C}$, unless otherwise specified under Conditions.

| Characteristics | | Conditions | min | typ | max | Unit |
|----------------------|--|--|-----|------|------|-------|
| UVLO _{VIN} | VIN Under Voltage Lock-Out | Rising threshold | | 2.5 | 3.0 | V |
| | | Hysteresis | | 200 | | mV |
| UVLO _{VCC} | VCC Under Voltage Lock-Out | Rising threshold | | 2.75 | 2.95 | V |
| | | Hysteresis | | 200 | | mV |
| V _{IL,EN} | EN input low threshold | | | | 0.9 | V |
| V _{IH,EN} | EN input high threshold | | 1.4 | | | V |
| V _{IL,PWM} | PWM input low threshold | | | | 0.6 | V |
| V _{IH,PWM} | PWM input high threshold | | 2.6 | | | V |
| V _{TRL,PWM} | PWM tri-state region | | 1.1 | | 2.1 | V |
| V _{HIZ,PWM} | PWM high impedance voltage | | | 1.6 | | V |
| I _{PWM} | PWM sink/source current | PWM = 0 V (source) | | 500 | | μA |
| | | PWM = 3.3 V (sink) | | -500 | | μA |
| t _{PWM} | PWM minimum pulse width | | | 15 | | ns |
| V _{O,ISEN} | TSEN voltage when fault | | 3.0 | 3.3 | | V |
| G _{TSEN} | TSEN gain | | | 8 | | mV/°C |
| O _{TSEN} | TSEN offset | T _J = +25 °C | | 800 | | mV |
| T _{TSEN} | TSEN overtemperature shutdown and fault flag | | | 160 | | °C |
| G _{ISEN} | ISEN gain | | | 5 | | μA/A |
| | | Accuracy | -2 | 0 | 2 | % |
| O _{ISEN} | ISEN offset | I _{out} = 0 A, V _{ISEN} = 1.2 V T _J = +25 °C | -4 | 0 | 4 | μA |
| V _{ISEN} | ISEN voltage range | | 0.7 | | 2.1 | V |
| I _{LIM,H} | High-side current limit | Threshold, cycle-by-cycle | | 120 | | A |
| | | Shutdown counter | | 10 | | Times |
| I _{LIM,L} | Low-side current limit | Threshold, cycle-by-cycle | | -50 | | A |
| | | No fault report Off time | | 200 | | ns |

Electrical specifications for BMR510X034/002 (V_{CC}=3.3V, without output capacitors) – Power Conversion

T_{P1} = -10 °C to 95 °C, V_{in} = 4.5 to 15 V, V_{CC} = 3.3 V, unless otherwise specified under Conditions.

Typical values given at: T_{P1} = +25 °C, V_{in} = 13.5 V, V_{out} = 0.8 V, I_{out} = 80 A, f_{sw} = 550 kHz, 2-phase single rail operation, otherwise specified under Conditions.

Measurements made on Reference board ROA 170 314.

External C_{in} = 1 x 270 µF/22 mΩ OSCON + 28 x 10 µF ceramic.

External C_{out} = 10 x 470 µF/3 mΩ POSCAP + 356 x 10 µF ceramic.

| Characteristics | | Conditions | min | typ | max | Unit |
|---------------------|------------------------------------|-------------------------------|-----|-----|-----|-------|
| V _{in} | Input supply | Continuous operation | 4.5 | | 15 | V |
| | | Peak | | | 16 | V |
| V _{CC} | Driver and logic supply | | 3.0 | 3.3 | 3.6 | V |
| V _{out} | Output voltage range | | 0.5 | | 1.3 | V |
| V _{out_ac} | Output ripple & noise | 20 MHz BW | | 2 | | mVp-p |
| f _{sw} | Switching frequency | T _{P1} = +25 °C | 500 | 550 | 600 | kHz |
| C _{in} | Internal input capacitance | V _I = 0 V | | 33 | | µF |
| L _{out} | Output inductance | I _O = 0 A | | 90 | | nH |
| I _{out} | Output current, peak | 2-phase operation | | | 160 | A |
| | | 1-phase operation | | | 80 | A |
| | Output current, continuous, Note 1 | 2-phase operation | 0 | 80 | | A |
| | | 1-phase operation | 0 | 40 | | A |
| I _{in} | V _{in} input current | Standby, EN = low | | 10 | | µA |
| I _{VCC} | V _{CC} input current | 1-phase operation | | 38 | | mA |
| | | I _{out} = 40 A | | | | |
| | | 2-phase operation | | 71 | | mA |
| | | I _{out} = 80 A | | | | |
| | | Standby, PWM1 = PWM2 = low | | 3 | | mA |

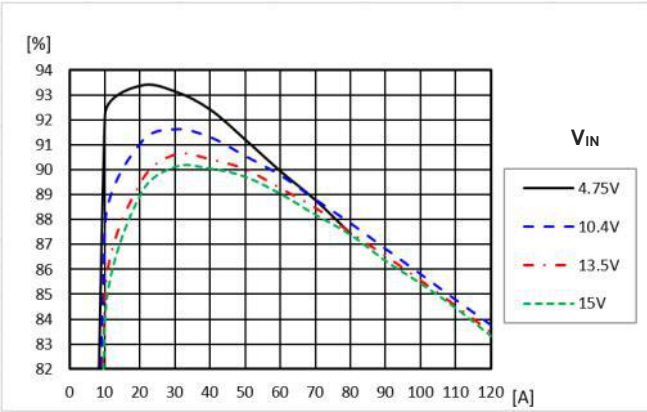
Note 1: The maximum continuous output current will also be limited by the thermal conditions.

See derating graphs and section Thermal Considerations.

Electrical graphs for BMR510X034/002

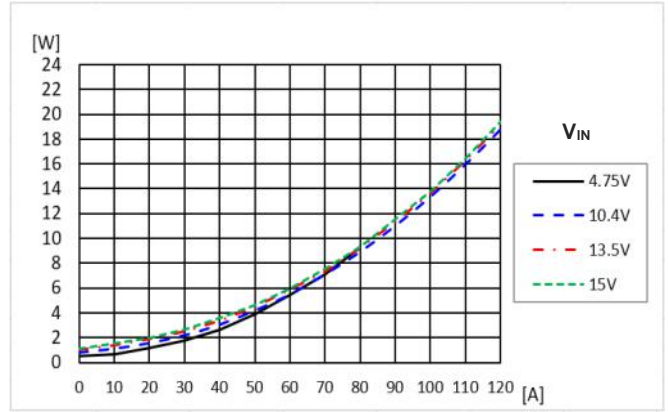
$V_{out} = 0.8 V$

Efficiency



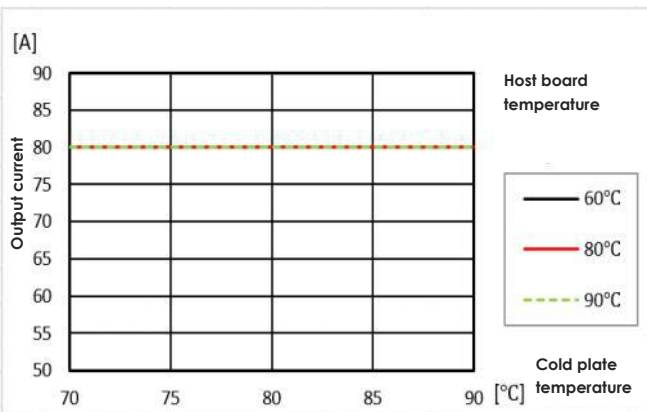
Efficiency vs. output current and input voltage
Driver losses excluded, 2 phases, $f_{sw} = 550KHz$

Power dissipation



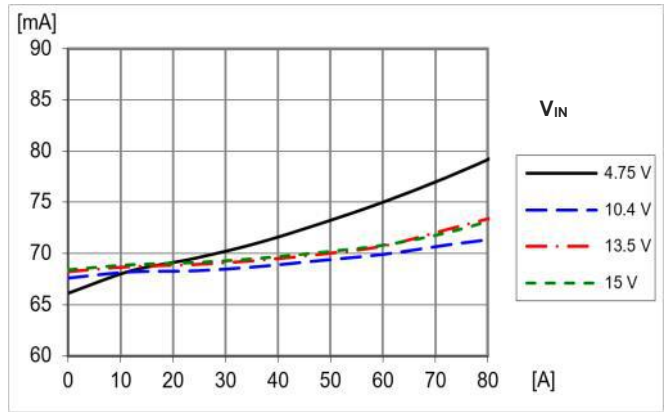
Dissipated power vs. output power
Driver losses excluded, 2 phases, $f_{sw} = 550KHz$

Output Current Derating



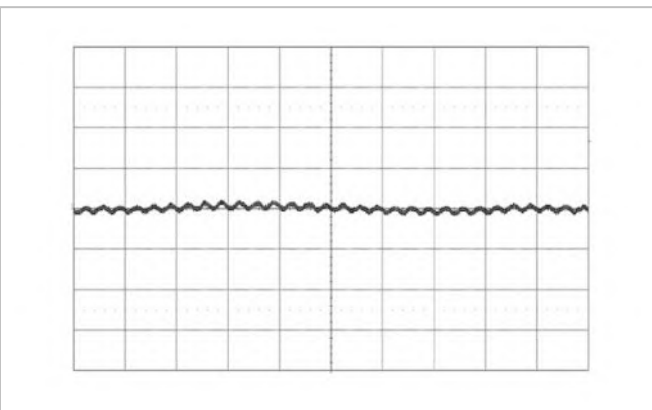
Thermal interface gap pad 0.5 mm, 3.5 W/mK. $V_{in} = 13.5 V$.

VCC input current



$V_{CC} = 3.3V$

Output ripple



$V_{in} = 13.5 V$, $I_{out} = 80 A$, Scale: 5 mV/div, 1.5 μs /div, 20 MHz BW. $C_{OUT} = 10 \times 470 \mu F / 3 m\Omega$ POSCAP + 365 \times 10 μF ceramic.

Electrical specifications for BMR510X04X/002 (VCC=5V, without output capacitors) — Control and Monitoring

$T_{P1} = -40\text{ °C}$ to 125 °C , $V_{in} = 12\text{ V}$, $V_{CC} = V_{EN} = 5\text{ V}$, unless otherwise specified under Conditions.

Typical values given at: $T_{P1} = +25\text{ °C}$, unless otherwise specified under Conditions.

| Characteristics | | Conditions | min | typ | max | Unit |
|----------------------|--|--|-----|------|------|-------|
| UVLO _{VIN} | VIN Under Voltage Lock-Out | Rising threshold | | 2.5 | 3.0 | V |
| | | Hysteresis | | 200 | | mV |
| UVLO _{VCC} | VCC Under Voltage Lock-Out | Rising threshold | | 2.75 | 2.95 | V |
| | | Hysteresis | | 200 | | mV |
| V _{IL,EN} | EN input low threshold | | | 1.0 | | V |
| V _{IH,EN} | EN input high threshold | | | 1.2 | | V |
| V _{IL,PWM} | PWM input low threshold | | | | 0.6 | V |
| V _{IH,PWM} | PWM input high threshold | | 2.6 | | | V |
| V _{TRL,PWM} | PWM tri-state region | | 1.1 | | 2.1 | V |
| V _{HIZ,PWM} | PWM high impedance voltage | | | 1.6 | | V |
| I _{PWM} | PWM sink/source current | PWM = 0 V (source) | | 500 | | μA |
| | | PWM = 3.3 V (sink) | | -500 | | μA |
| t _{PWM} | PWM minimum pulse width | | | 15 | | ns |
| V _{O,ISEN} | TSEN voltage when fault | | 3.0 | 3.3 | | V |
| G _{TSEN} | TSEN gain | | | 8 | | mV/°C |
| O _{TSEN} | TSEN offset | T _J = +25 °C | | 800 | | mV |
| T _{TSEN} | TSEN overtemperature shutdown and fault flag | | | 165 | | °C |
| G _{ISEN} | ISEN gain | | | 5 | | μA/A |
| | | Accuracy | -2 | 0 | 2 | % |
| O _{ISEN} | ISEN offset | I _{out} = 0 A, V _{ISEN} = 1.2 V T _J = +25 °C | -4 | 0 | 4 | μA |
| V _{ISEN} | ISEN voltage range | | 0.7 | | 2.1 | V |
| I _{LIM,H} | High-side current limit | Threshold, cycle-by-cycle | | 130 | | A |
| | | Shutdown counter | | 10 | | Times |
| I _{LIM,L} | Low-side current limit | Threshold, cycle-by-cycle | | -50 | | A |
| | | No fault report | | | | |
| | | Off time | | 200 | | ns |

Electrical specifications for BMR510X044/002 (V_{CC}=5 V, without output capacitors) – Power Conversion

T_{P1} = -10 °C to 95 °C, V_{in} = 4.5 to 15 V, V_{CC} = 5 V, unless otherwise specified under Conditions.

Typical values given at: T_{P1} = +25 °C, V_{in} = 13.5 V, V_{out} = 0.75 V, I_{out} = 80 A, f_{sw} = 550 kHz, 2-phase single rail operation, otherwise specified under Conditions.

Measurements made on Reference board ROA 170 314.

External C_{in} = 1 x 270 µF/22 mΩ OSCON + 28 x 10 µF ceramic.

External C_{out} = 10 x 470 µF/3 mΩ POSCAP + 356 x 10 µF ceramic.

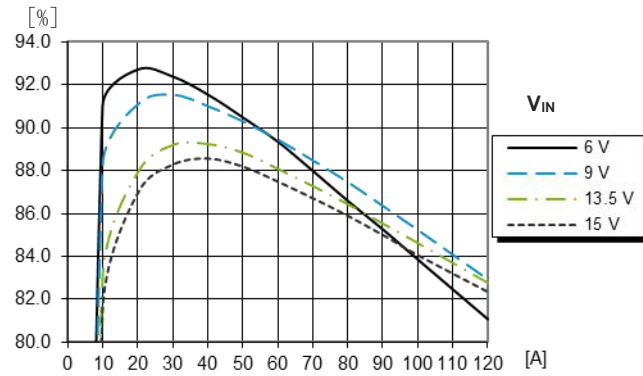
| Characteristics | | Conditions | min | typ | max | Unit |
|---------------------|------------------------------------|-------------------------------|-----|-----|-----|-------|
| V _{in} | Input supply | Continuous operation | 6 | | 15 | V |
| | | Peak | | | 16 | V |
| V _{CC} | Driver and logic supply | | 4.5 | 5 | 5.5 | V |
| V _{out} | Output voltage range, | | 0.5 | | 1.8 | V |
| V _{out_ac} | Output ripple & noise | 20 MHz BW | | 2 | | mVp-p |
| f _{sw} | Switching frequency | T _{P1} = +25 °C | 500 | 550 | 600 | kHz |
| C _{in} | Internal input capacitance | V _{in} = 0 V | | 33 | | µF |
| L _{out} | Output inductance | I _{out} = 0 A | | 90 | | nH |
| I _{out} | Output current, peak | 2-phase operation | | | 160 | A |
| | | 1-phase operation | | | 80 | A |
| | Output current, continuous, Note 1 | 2-phase operation | 0 | 80 | | A |
| | | 1-phase operation | 0 | 40 | | A |
| I _{in} | V _{in} input current | Standby, EN = low | | 10 | | µA |
| I _{vcc} | V _{CC} input current | 1-phase operation | | 28 | | mA |
| | | I _{out} = 40 A | | | | |
| | | 2-phase operation | | 52 | | mA |
| | | I _{out} = 80 A | | | | |
| | | Standby, PWM1 = PWM2 = low | | 4.5 | | mA |

Note 1: The maximum continuous output current will also be limited by the thermal conditions.

Electrical graphs for BMR510X044/002

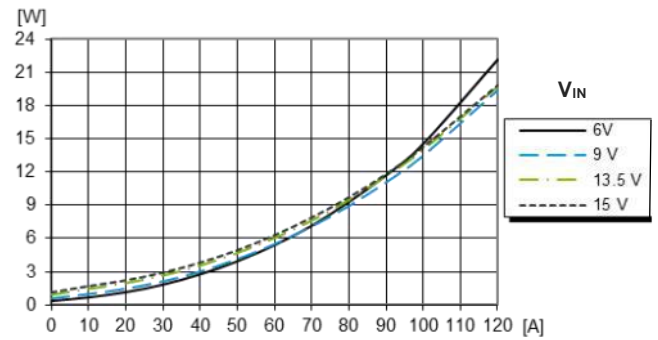
$V_{out} = 0.75 V$

Efficiency



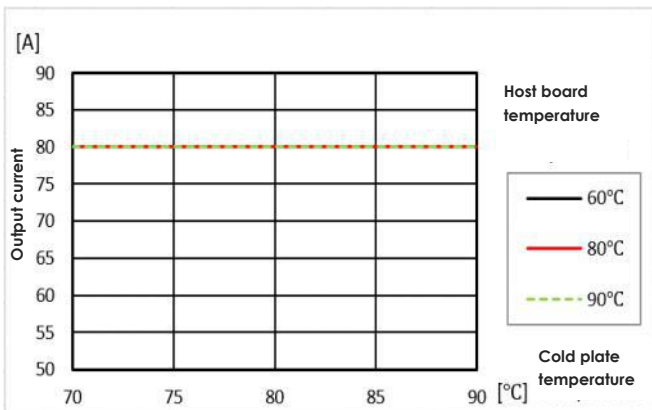
Efficiency vs. output current and input voltage
Driver losses excluded, 2 phases, fsw=550KHz

Power dissipation



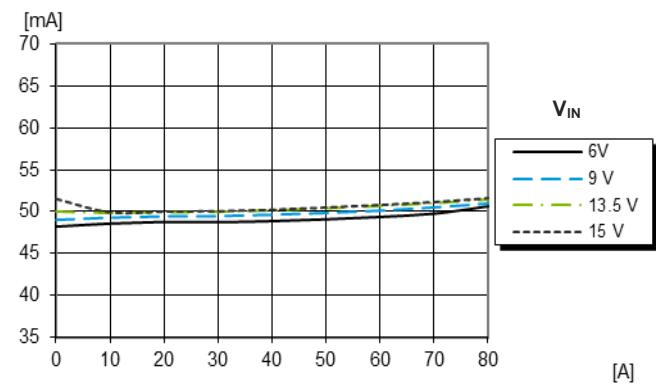
Dissipated power vs. output power
Driver losses excluded, 2 phases, fsw= 550KHz

Output Current Derating



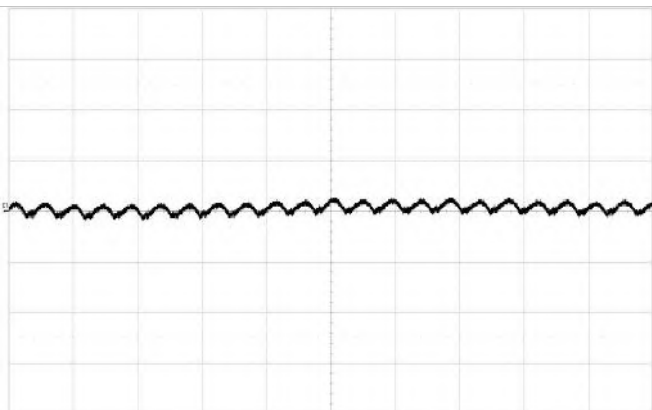
Gap pad between baseplate and test board 1mm 3W/m-K.
Gap pad between module and cold plate 0.5mm 10W/m-K

VCC input current



VCC=5V, Fs=550KHz

Output ripple



$V_{in} = 13.5 V$, $I_o = 80 A$, Scale: 5 mV/div, 1.5 µs/div, 20 MHz BW. $C_{out} = 10 \times 470 \mu F / 3 m\Omega$ POSCAP + 365 x 10 µF ceramic.

Electrical specifications for BMR510X041/002 (V_{CC} = 5 V, with 24 output capacitors)**Power Conversion**

$T_{P1} = -10\text{ °C}$ to 95 °C , $V_{in} = 6$ to 15 V , $V_{CC} = 5\text{ V}$, unless otherwise specified under Conditions.

Typical values given at: $T_{P1} = +25\text{ °C}$, $V_{in} = 13.5\text{ V}$, $V_O = 0.75\text{ V}$, $I_{out} = 80\text{ A}$, $f_{sw} = 500\text{ kHz}$, 2-phase single rail operation, otherwise specified under Conditions.

Measurements made on Reference board ROA 170 323.

External $C_{in} = 1 \times 270\text{ }\mu\text{F}/22\text{ m}\Omega$ OSCON + $28 \times 10\text{ }\mu\text{F}$ ceramic.

External $C_{out} = 10 \times 470\text{ }\mu\text{F}/3\text{ m}\Omega$ POSCAP + $356 \times 10\text{ }\mu\text{F}$ ceramic.

| Characteristics | | Conditions | min | typ | max | Unit |
|-----------------|-------------------------------------|--|-----|-----|-----|---------------|
| V_{in} | Input supply | Continuous operation | 6 | | 15 | V |
| | | Peak | | | 16 | V |
| V_{CC} | Driver and logic supply | | 4.5 | 5 | 5.5 | V |
| V_{out} | Output voltage range | | 0.5 | | 1.8 | V |
| V_{out_ac} | Output ripple & noise | 20 MHz BW | | 2 | | mVp-p |
| f_{sw} | Switching frequency | $T_{P1} = +25\text{ °C}$ | 450 | 500 | 550 | kHz |
| C_{in} | Internal input capacitance | $V_{in} = 0\text{ V}$ | | 33 | | μF |
| C_{out} | Internal output capacitance, Note 2 | $V_{out} = 0\text{ V}$ | | 528 | | μF |
| L_{out} | Output inductance | $I_{out} = 0\text{ A}$ | | 87 | | nH |
| I_{out} | Output current, peak | 2-phase operation | | | 160 | A |
| | | 1-phase operation | | | 80 | A |
| | Output current, continuous, Note 1 | 2-phase operation | 0 | 80 | | A |
| | | 1-phase operation | 0 | 40 | | A |
| I_{in} | V_{in} input current | Standby, EN = low | | 10 | | μA |
| I_{VCC} | V_{CC} input current | 1-phase operation $I_{out} = 40\text{ A}$ | | 28 | | mA |
| | | 2-phase operation $I_{out} = 80\text{ A}$ | | 52 | | mA |
| | | Standby, PWM1 = PWM2 = low | | 4.5 | | mA |

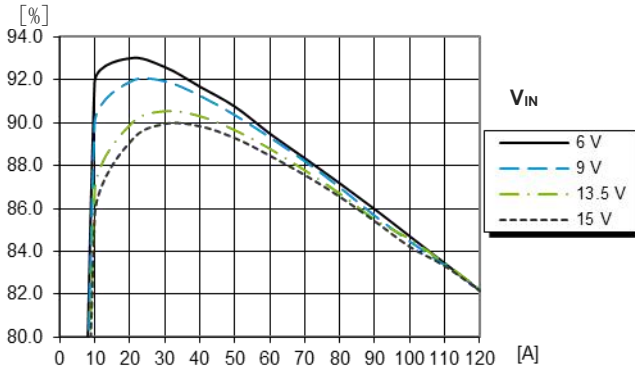
Note 1: The maximum continuous output current will also be limited by the thermal conditions.

Note 2: 24 pcs 22 μF MLCC

Electrical graphs for BMR510X041/002

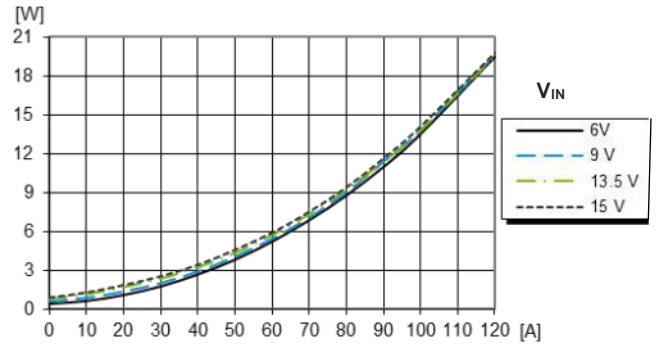
$V_{out} = 0.75 V$

Efficiency



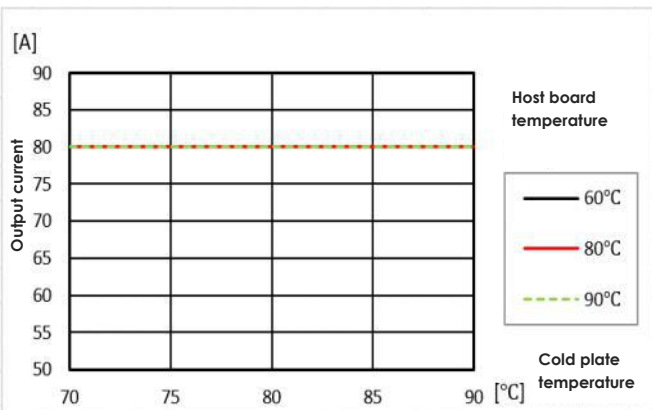
Efficiency vs. output current and input voltage
Driver losses excluded, 2 phases, fsw=500KHz

Power dissipation



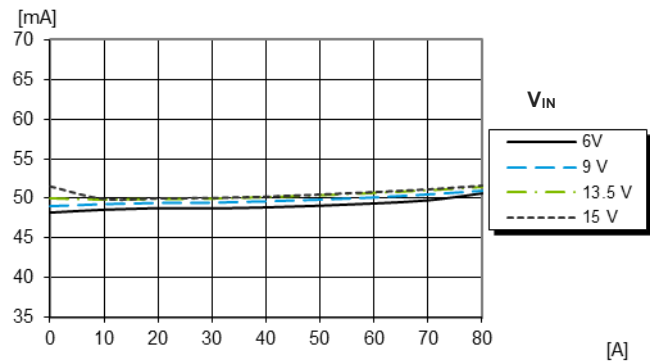
Dissipated power vs. output power
Driver losses excluded, 2 phases, fsw= 500KHz

Output Current Derating

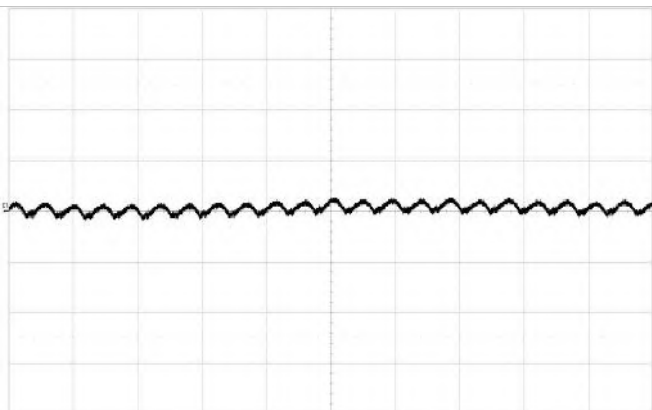


Thermal interface gap pad 0.5 mm, 10 W/mK. $V_{in} = 13.5 V$.

VCC input current



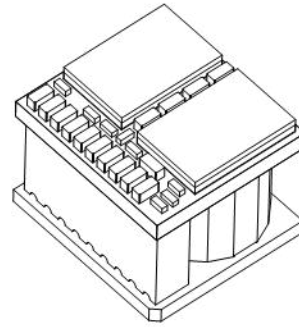
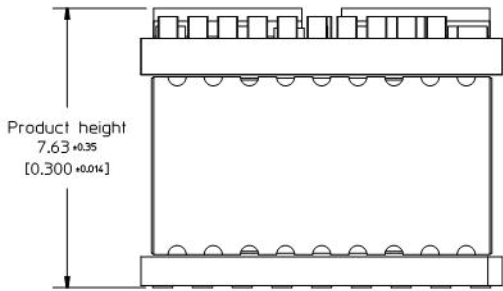
$V_{cc} = 5V$, fsw=500KHz



$V_{in} = 13.5 V$, $I_{out} = 80 A$, Scale: 2 mV/div, 2μs/div, 20 MHz BW. $C_{out} = 10 \times 470 \mu F / 3 m\Omega$ POSCAP + 365 x 10 μF ceramic.

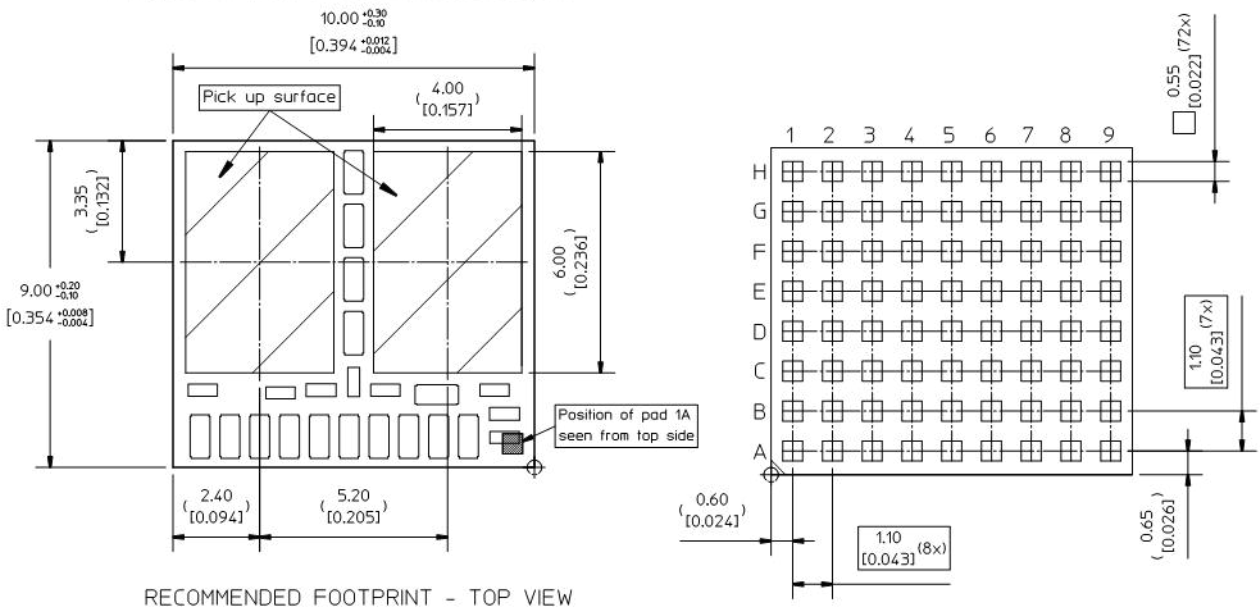
Part 2: Mechanical information

BMR5101034/002, BMR5101044/002: Surface Mount Version

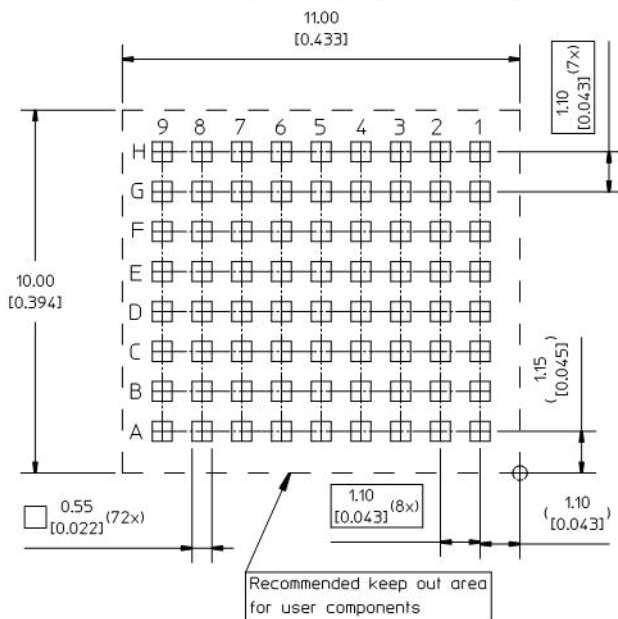


TOP VIEW

Pin position acc. to recommended footprint



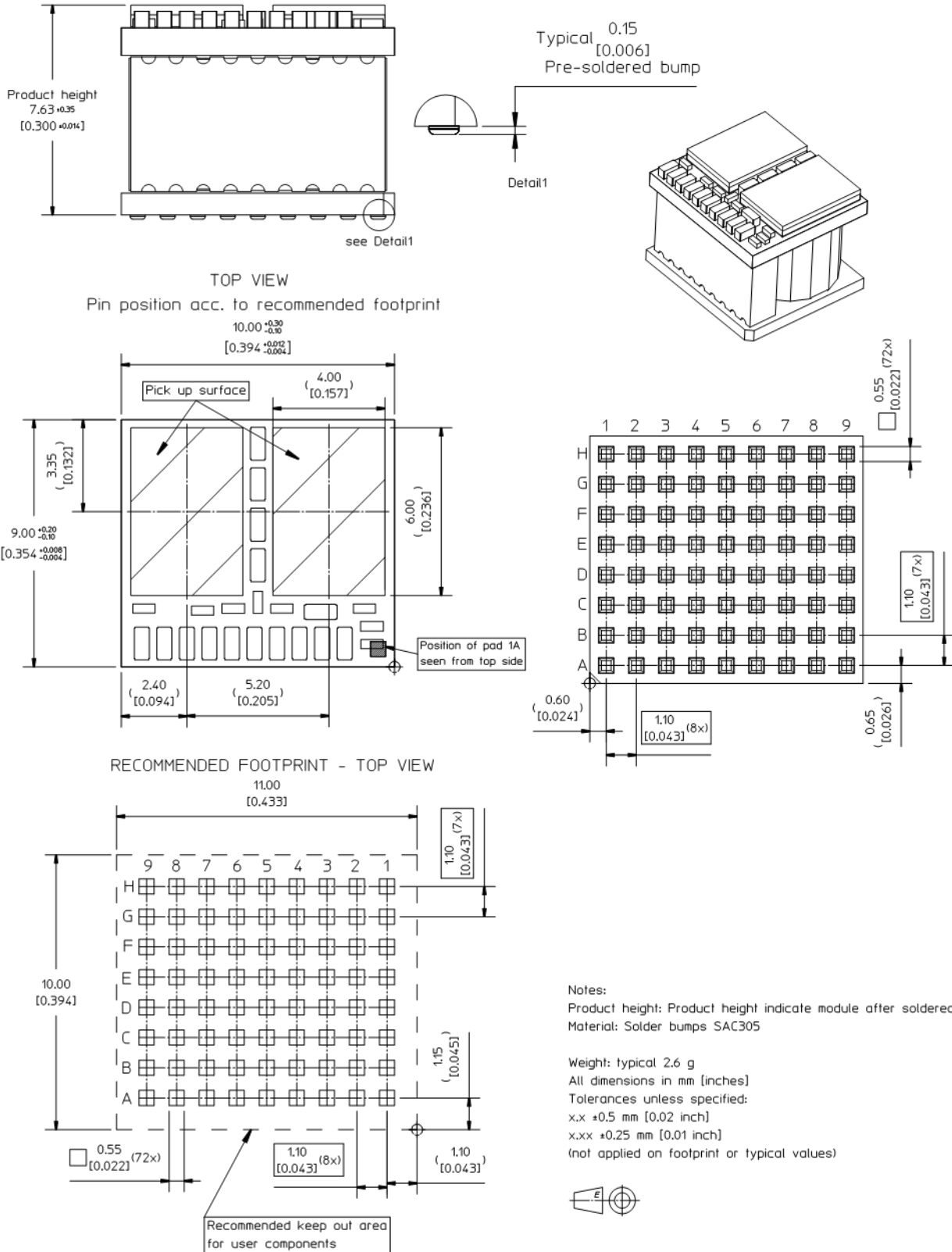
RECOMMENDED FOOTPRINT - TOP VIEW



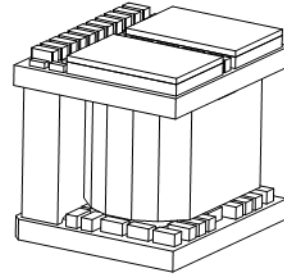
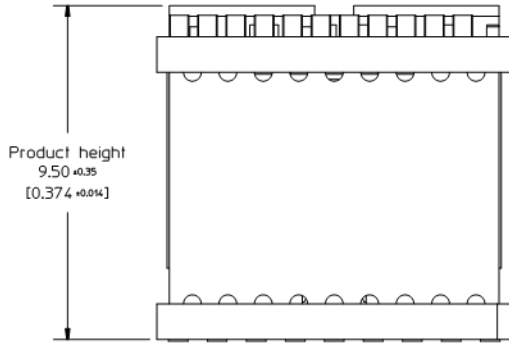
Weight: typical 2.6 g
All dimensions in mm [inches]
Tolerances unless specified:
x.x ±0.5 mm [0.02 inch]
x.xx ±0.25 mm [0.01 inch]
(not applied on footprint or typical values)



BMR5100034/002, BMR5100044/002: Surface Mount Version with solder bumps

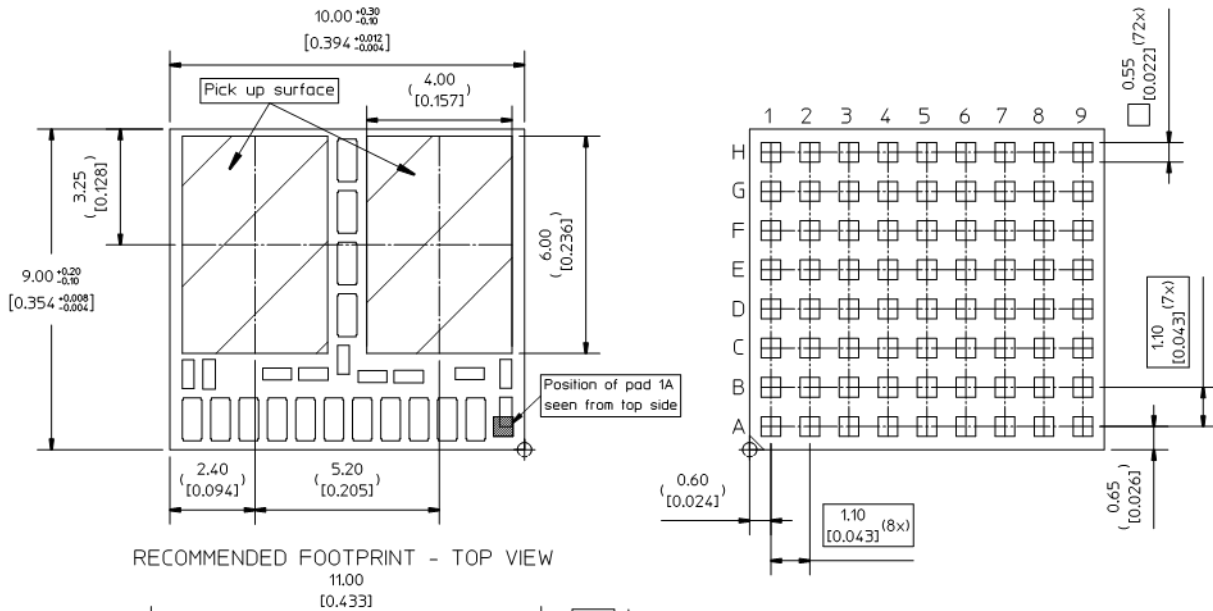


Part 2: Mechanical information
BMR5101041/002: Surface Mount Version

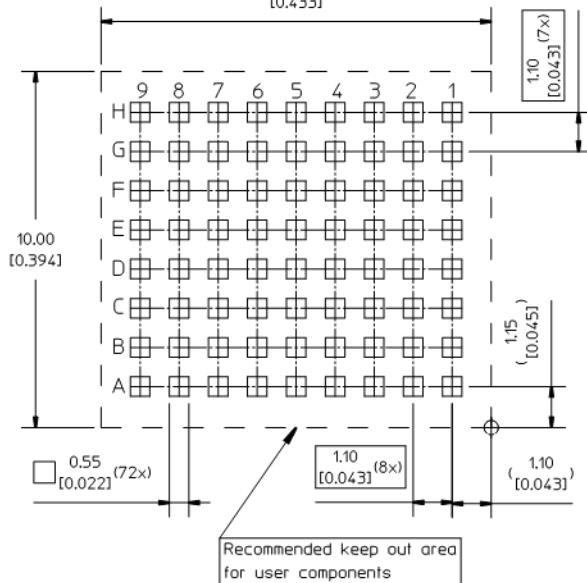


TOP VIEW

Pin position acc. to recommended footprint



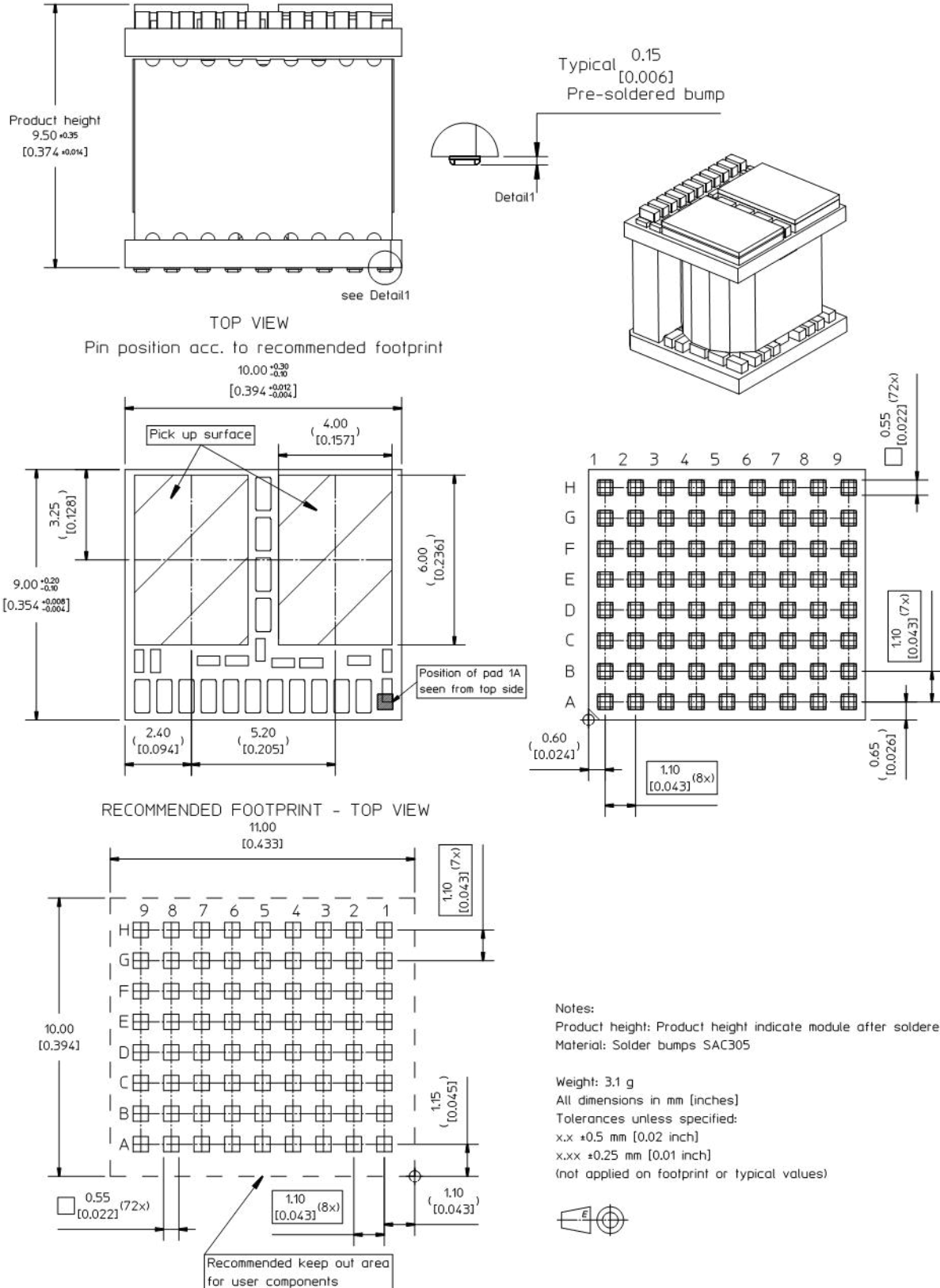
RECOMMENDED FOOTPRINT - TOP VIEW
11.00
[0.433]



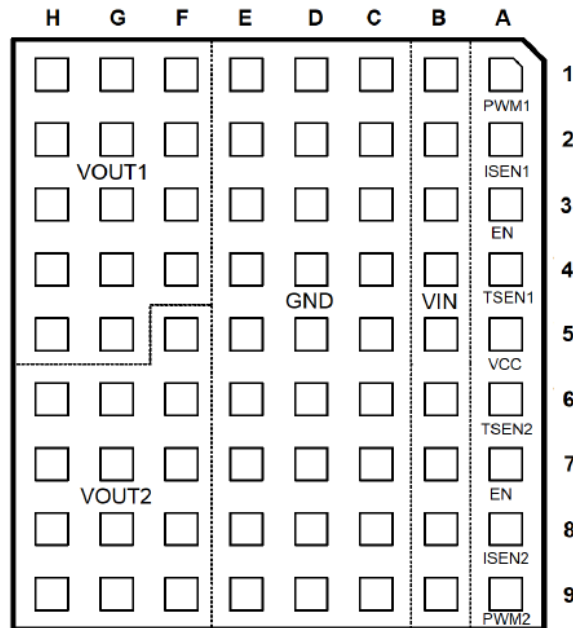
Weight: 3.1 g
All dimensions in mm [inches]
Tolerances unless specified:
x.x ±0.5 mm [0.02 inch]
x.xx ±0.25 mm [0.01 inch]
(not applied on footprint or typical values)



BMR5100041/002: Surface Mount Version with solder bumps



Connections



Pin layout, top view

| Pin | Designation | Type | Function |
|-----------------------|-------------|--------|--|
| A1 | PWM1 | Input | Pulse-width modulation input, phase 1. The PWM1 signal shall be 180° phase shifted compared to the PWM2 signal. |
| A2 | ISEN1 | Output | Current sense output , phase 1. Use external resistor to adjust the voltage proportional to the inductor current . |
| A3, A7 | EN | Input | Active high enable input, common for phase 1 and 2. |
| A4 | TSEN1 | Output | Temperature sense and fault reporting, phase 1. |
| A5 | VCC | Input | Driver and internal circuitry supply. Connect to +3.3 V. |
| A6 | TSEN2 | Output | Temperature sense and fault reporting, phase 2. |
| A8 | ISEN2 | Output | Current sense output, phase 2. Use external resistor to adjust the voltage proportional to the inductor current. |
| A9 | PWM2 | Input | Pulse-width modulation input, phase 2. The PWM2 signal shall be 180° phase shifted compared to the PWM1 signal. |
| B1-B9 | VIN | Power | Input voltage. |
| C1-C9, D1-D9 E1-E9 | GND | Power | Power ground and digital ground. |
| F1-F4, G1-G5 H1-H5 | VOUT1 | Power | Output voltage, phase 1. |
| F5-F9, G6-G9 H6-H9 | VOUT2 | Power | Output voltage, phase 2. |

Part 3: Thermal considerations

Thermal Consideration

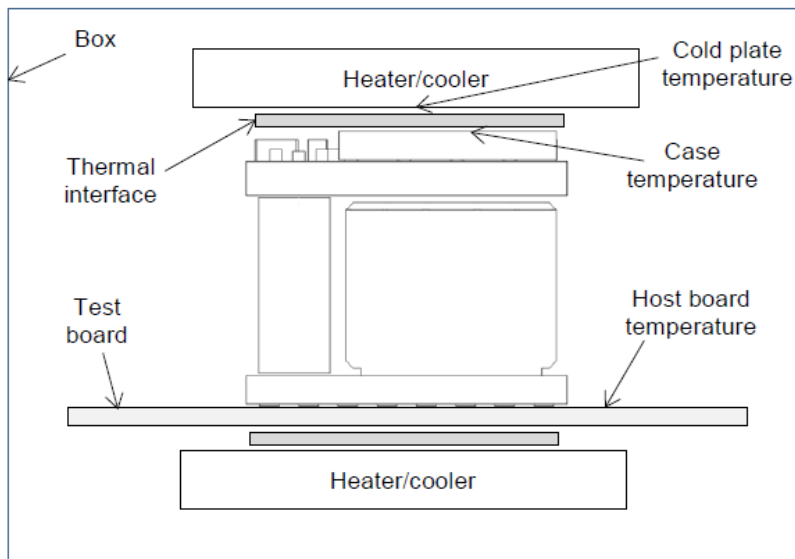
General

The product is designed with power switches on top. To operate with top side cooling towards a heatsink or a cold plate. This is required to handle operation with high load. Cooling is also achieved by conduction to the host board and surrounding air. Sufficient cooling must be provided to ensure reliable operation.

The Output Current Derating graph found in the [Electrical Specification section](#) provides the available output current versus cold plate temperature and host board temperature.

Test Setup – Cold Plate

The product is tested in a box with two heater/coolers; one as a cold plate to control the temperature at the top of the module, another on the bottom side of the test board to control the host board temperature. The test board used is 105 x 157 mm in size with 1.6 mm thickness and 4 layers of 2 oz.



Test setup — Cold plate

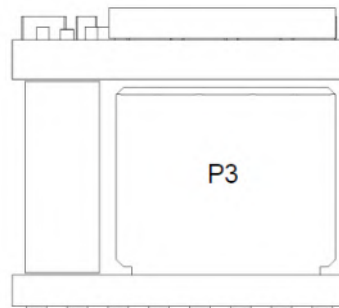
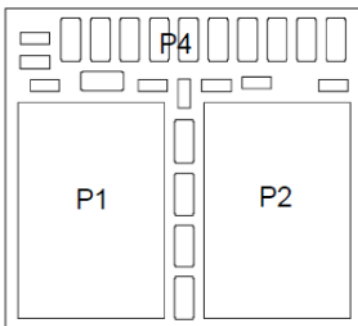
Definition of Product Operating Temperature

The temperature at positions P1-P4 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperature above specified maximum measured at the specified position is not allowed and may cause permanent damage.

Note that the maximum value is the maximum operating temperature and that the provided [Electrical Specification](#) data is guaranteed up to $T_{P1} = +95\text{ °C}$.

Part 3: Thermal considerations

| Position | Description | Max temperature |
|----------|---|------------------------------|
| P1 | Power switch case phase 1 reference point | $T_{P1}=125^{\circ}\text{C}$ |
| P2 | Power switch case phase 2 | $T_{P2}=125^{\circ}\text{C}$ |
| P3 | M1, Inductor core | $T_{P3}=125^{\circ}\text{C}$ |
| P4 | Capacitors | $T_{P4}=105^{\circ}\text{C}$ |

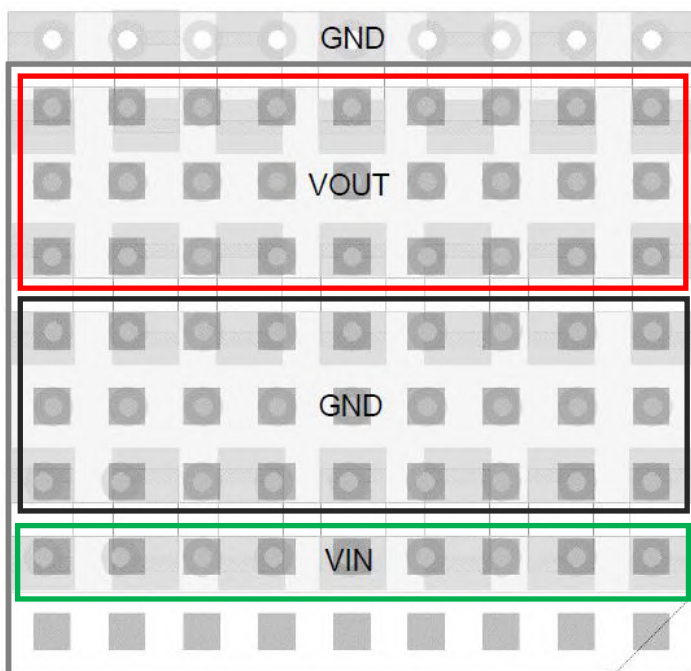


Part 4: PCB layout considerations

PCB Layout Consideration

1. The radiated EMI performance of the product will depend on the PCB layout and ground layer design. Ground planes shall be used to increase the stray capacitance in the PCB and improve the high frequency EMC performance. The ground plane shall connect to the GND pins of the devices and the equipment ground or chassis.
2. For a multiphase rail including several power modules, layout should be as symmetrical as possible in order to help balance the current between devices.
3. If possible, use planes on several layers to carry V_{in} , V_{out} and ground. There should be an adequate number of vias close to the V_{in} , V_{out} and GND pins to lower input and output impedances and improve heat spreading between the product and the host board.
4. Care should be taken in the routing of the ISEN and TSEN connections. The routing should be along a GND plane and should avoid areas of switching signals or high electric or magnetic fields, e.g. keep away from PWM signals.
5. The external input capacitors, C_{in_EXT} , shall be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See [AN323](#) for more details.
6. The external output capacitors, C_{out_EXT} , should be placed close to the output pins to handle the output current ripple, and close to the load to handle the load transients. See [AN321](#) for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.

Below picture shows a layout example where the module is mounted on the top side of the PCB and 7 pcs 0603 input capacitors and 14 pcs 0603 output capacitors are placed on the bottom side of the PCB, providing a short connection to the VIN, VOUT and GND pins through vias in module pads.

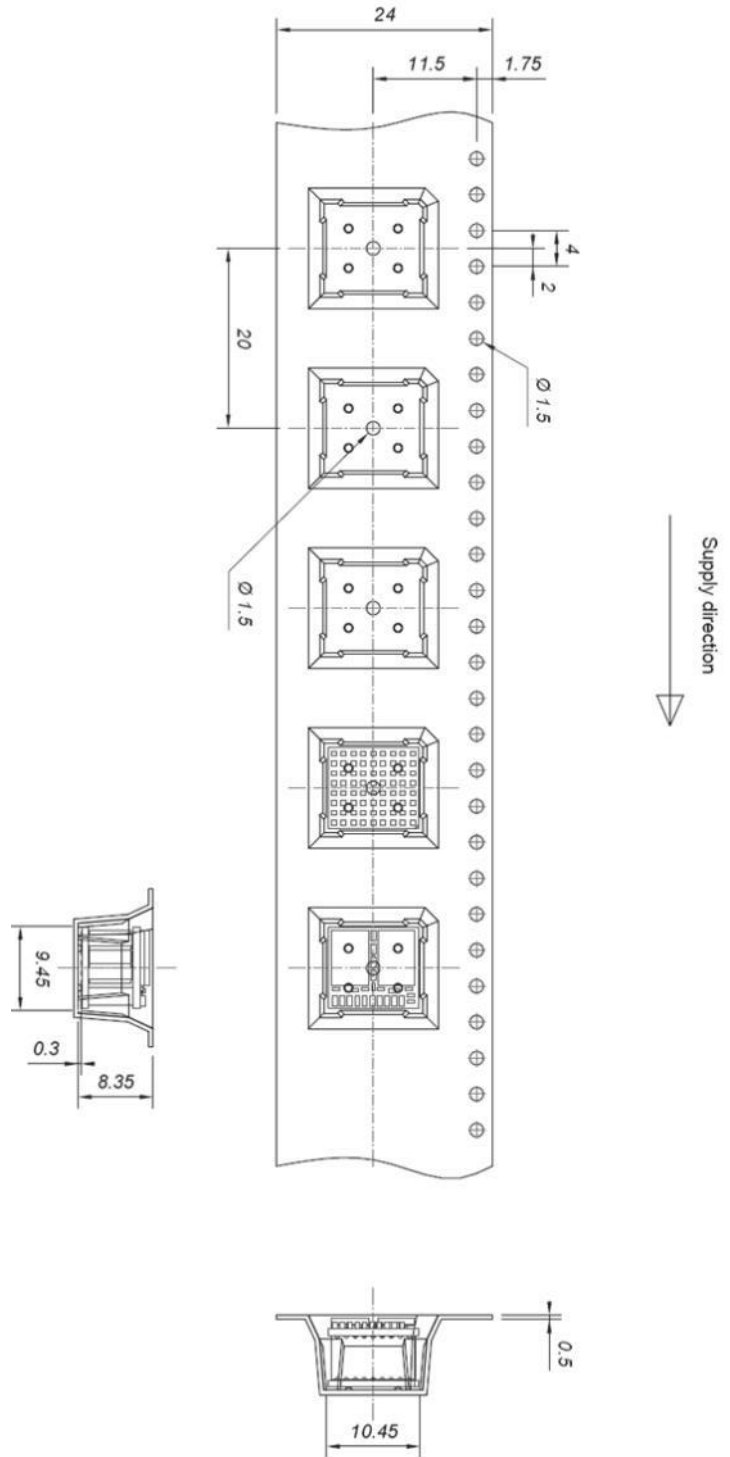


Layout example: Input and output capacitors' placement close to the module (top view).

Part 5: Packaging

Packaging information— BMR510XXX4 (7.63 mm height without output capacitors)

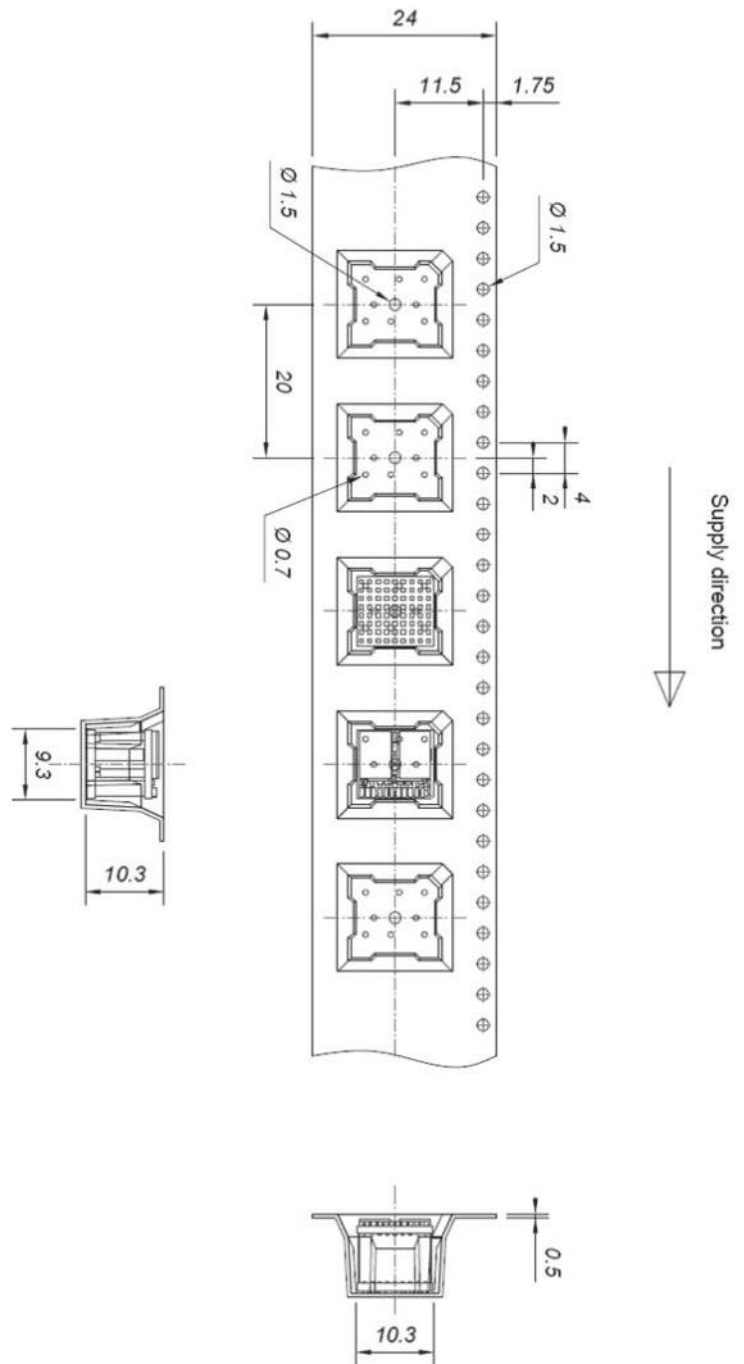
| C option: | |
|------------------------------|--------------------------------------|
| Material | Black Conductive Polystyrene |
| Surface resistance | $10^5 < \text{ohm/square} < 10^{11}$ |
| Bakability | The tape is not bakeable |
| Tape width, W | 24 mm [0.95 inch] |
| Pocket pitch, P ₁ | 20 mm [0.79 inch] |
| Pocket depth, K ₀ | 8.35 mm [0.33 inch] |
| Reel diameter | 330 mm [13.0 inch] |
| Reel capacity | 350 products /reel |
| Reel weight | 1450 g/full reel |



Part 5: Packaging

Packaging information— BMR510XX41(9.5 mm height with 24 output capacitors)

| C option: | |
|------------------------------------|--------------------------------------|
| Material | Black Conductive Polystyrene |
| Surface resistance | $10^5 < \text{ohm/square} < 10^{11}$ |
| Bakability | The tape is not bakeable |
| Tape width, W | 24 mm [0.95 inch] |
| Pocket pitch, P₁ | 20 mm [0.79 inch] |
| Pocket depth, K₀ | 10.3 mm [0.41 inch] |
| Reel diameter | 330 mm [13.0 inch] |
| Reel capacity | 250 products /reel |
| Reel weight | 1300 g/full reel |



Part 6: Revision history

Revision table

| Revision number | revision change | date | revisor |
|-----------------|--|------------|----------|
| Rev. A | New document | 2022/12/21 | JIDDAYUE |
| Rev. B-D | Formatting updates | 2023/01/10 | KARTWAER |
| Rev. E | Add new variants BMR510X041 and BMR510X044 | 2024/11/27 | JIDDIYAN |
| | | | |

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The information and specifications in this datasheet is believed to be correct at the time of publication. However, no liability is accepted for inaccuracies, printing errors or for any consequences thereof. Flex reserves the right to change the contents of this technical specification at any time without prior notice.

TECHNICAL REFERENCE DOCUMENT: GENERAL INFORMATION

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the *RoHS directive 2011/65/EU* and *2015/863* have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, DIBP and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power Modules products are found in the [Statement of Compliance document](#).

Flex Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals ([REACH](#)) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality statement

The products are designed and manufactured in an industrial environment where quality systems and methods like [ISO 9001](#), [ISO 14001](#), [ISO 45001](#), *Six Sigma*, and *SPC* are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged workforce, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in *Flex Power Modules' General Terms and Conditions of Sales*.

Limitation of Liability

Flex Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Product qualification specifications

| Characteristics | | | |
|---|--|--|---|
| External visual inspection | IPC-A-610 | | |
| Temperature shock test (Temperature cycling) | IEC 60068-2-14 Na | Temperature range Number of cycles Dwell/transfer time | -40 to 125°C 700 15 min/0-1 min |
| Cold (in operation) | IEC 60068-2-1 Ad | Temperature T _A Duration | -45°C 72 hr |
| Damp heat | IEC 60068-2-67 Cy | Temperature Humidity Duration | 85°C 85% RH 1000 hr |
| Dry heat | IEC 60068-2-2 Bd | Temperature Duration | 125°C 1000 hr |
| Electrostatic discharge susceptibility | IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115 | Human body model (HBM) Machine Model (MM) | Class 2, 2000 V Class 3, 200 V |
| Immersion in cleaning solvents | IEC 60068-2-45 XA, method 2 | Water Fluxcleaner Isopropyl alcohol | 55°C 23° C 35°C |
| Mechanical shock | IEC 60068-2-27 Ea | Peak acceleration Duration | 100 g 6 ms |
| Moisture classification and reflow sensitivity ¹ | J-STD-020E | Level 3 (Pb Free) | 245°C |
| Operational Life test Rapid Temp. | MIL-STD-202G, method 108A | Duration | 1000 hr |
| Robustness of terminations | IEC 60068-2-21 Test Ue1 | Surface mount products | All leads |
| Solderability (surface mount) | IEC 60068-2-58 test T _d | Preconditioning Temperature, Pb-free | Steam ageing 245°C |
| Vibration, broad band random | IEC 60068-2-64 Fh, method 1 | Frequency Spectral density Duration | 10 to 500 Hz 0.07 g ² /Hz 10 min in each direction |

Note 1: only for products intended for reflow soldering (surface mount products & pin-in paste products)

TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

Operating Information

BMR 510 is a two-phase non-isolated high-efficiency small footprint step-down power block. It includes drivers, MOSFETs, output inductors and sensing circuitry for output currents and junction temperatures. Further, it includes over-current and over-temperature protection functions with fault reporting. The product has two independent outputs, which can be used separately (dual rail) or in parallel (single rail dual phase). Several products can be paralleled for multiphase operation.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage during large load transients.

It is recommended to use at least 70 μF ceramic external input capacitors for each module, placed closed to input pins and with low impedance connections to the VIN and GND pins to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors

The output capacitor requirement depends on two considerations: output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to minimize output voltage deviation.

It is recommended to place at least 140 μF ceramic capacitors close to each product, since it has no internal output capacitance. In addition, low ESR ceramic and low ESR electrolytic/polymer capacitors shall be placed as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts for capacitance to be effective.

See application note AN321 for further guidelines on how to choose and apply output capacitors.

TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

Enable

When the voltages at VIN and VCC pins are sufficiently high and the EN pin is high, operation begins. The EN pins are connected together in the product and common to both phases.

Pulse-Width Modulation (PWM)

The pulse-width modulation input pins are capable of tri-state input. When the PWM input is high, the high-side MOSFET is turned on and the low-side MOSFET is turned off. When the PWM input is low, the high-side MOSFET is turned off and the low-side MOSFET is turned on. If the PWM input is floated, it will force the PWM into tri-state.

When the PWM input signal is within the tri-state threshold window for a typical 40 ns, the high-side MOSFET turns off immediately, and the low-side MOSFET enters diode emulation mode, which is on until zero-current detection.

The tri-state PWM input can come from a forced mid-voltage PWM signal or made by floating the PWM input. The internal current source charges the signal to a middle voltage.

When operating both phases of the product, PWM1 and PWM2 pulses shall be 180° shifted.

Diode Emulation Mode

In diode emulation mode, when PWM is in a tri-state input, the low side MOSFET is turned on whenever the inductor current is positive. The low side MOSFET turns off if the inductor current is negative or after the inductor current crosses the zero current.

Current Sense

The ISEN pins are bidirectional current source outputs proportional to the inductor current of each phase. The gain is 5 $\mu\text{A}/\text{A}$. An external resistor must be used to program the voltage gain proportional to the inductor current, if needed.

The ISEN outputs have two states. In disable mode (EN = low), the current sense circuit is disabled and the ISEN outputs are in the high impedance state.

| EN | ISEN |
|------|--------|
| High | Active |
| Low | Hi-Z |

The voltage of the ISEN pins must be within the specified voltage range to achieve an accurate current reporting. In general, there is a resistor, RIOUT, connected from ISEN to a reference voltage, VCM, that can sink small currents to provide enough voltage level to meet the required operating voltage range. Proper VCM and RIOUT values can be determined by the equation:

$$0.7 \text{ V} < (I_{\text{ISEN}} \times R_{\text{IOUT}}) + V_{\text{CM}} < 2.1 \text{ V}$$

TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

The current sense outputs can be used by the controller to monitor the output current accurately. The cycle-by-cycle current information from the ISEN pins can be used for phase-current balancing, over-current protection, and voltage positioning (output voltage droop).

Current Limit

When high side over-current is detected, the high side MOSFET turns off for that PWM cycle. If there are ten consecutive cycles of a high side current limit event, the high side MOSFET latches off, TSEN pulls high to VCC, and the low side MOSFET turns on until zero current detection. Toggle EN or recycle VIN or VCC to release the latch and restart operation.

When the low side under-current is detected (negative current) the low side MOSFET is turned off and the high side MOSFET is turned on for 200 ns to limit the negative current cycle by cycle. The low side negative current limit will not trigger a fault report.

Temperature Sense with Fault Indicator

The TSEN pins have two functions:

1. Junction temperature sense.
2. Fault detection.

The voltage at the TSEN pin is proportional to the junction temperature whenever VIN and VCC is higher than their UVLO thresholds. The gain is 8 mV/°C and has an 800 mV offset at 25 °C. Examples:

$$V_{TSEN} = 0.8 \text{ V @ } T_J = 25 \text{ °C}$$

$$V_{TSEN} = 1.6 \text{ V @ } T_J = 125 \text{ °C}$$

When any fault occurs, TSEN is pulled to the VCC voltage to report the fault event, regardless of the current junction temperature. 200 ns after the fault has occurred, the PWM impedance changes accordingly to indicate the fault type:

| Fault Type | PWM Impedance |
|-----------------------------------|---------------|
| Over-current limit protection | 10 kΩ to GND |
| Over-temperature limit protection | 20 kΩ to GND |
| Internal short protection | 1 kΩ to VCC |

For multiphase operation, connect TSEN of each phase together to report the highest junction temperature. It is recommended to add a filter to the TSEN signal. See Application Example for typical component values to use.

Temperature Limit

When the over-temperature threshold is exceeded, the high side MOSFET latches off, TSEN pulls high to VCC, and the low side MOSFET turns on until zero current detection. Toggle EN or recycle VIN or VCC to release the latch and restart operation.

TECHNICAL REFERENCE DOCUMENT: SOLDERING

Soldering Information — Surface mounting

Products intended for surface mount assembly are qualified for use in a Pb-free forced convection or vapor phase reflow soldering process.

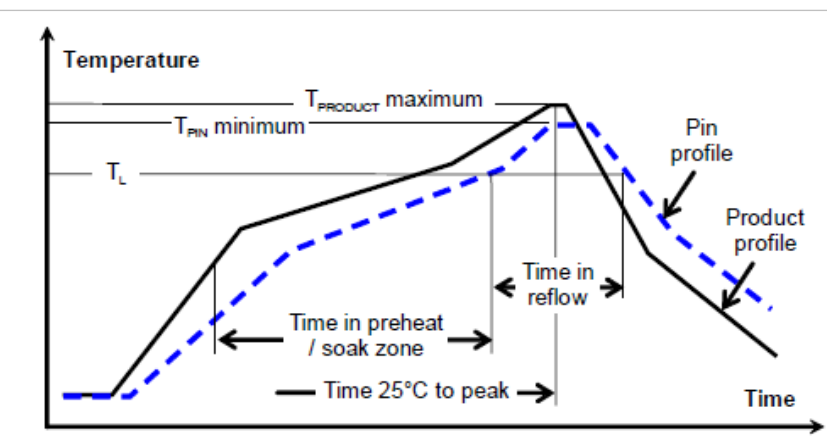
The surface mount product is intended for forced convection or vapor phase reflow soldering in Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

T_L is the typical solder melting (liquidous) temperature
 $T_{product}$ is measured on the power module's hotspot
 T_{pin} is measured on the power module output power pins' solder joints at the customer board

| General reflow process specification | | Pb-free, SAC305 |
|--|---------------|-----------------|
| Average ramp-up rate ($T_{product}$) | | 3 °C/s max |
| Typical solder melting temp. | T_L | 221° C |
| Min/Max. reflow time above T_L | T_{pin} | 60 –150 s |
| Min. pin temp. | T_{pin} | 235 °C |
| Peak product temp. | $T_{product}$ | 245 °C |
| Average ramp-down ($T_{product}$) | | 6°C/s max |
| Max. time 25° C to peak | | 8 minutes |



Typical soldering profile

Pb-free solder classification

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020E.

Products reflow processes - Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{MIN}) in excess of the solder melting temperature (T_L , 217 to 221 °C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235 °C on all solder joints is recommended to ensure a reliable solder joint

During reflow $T_{PRODUCT}$ must not exceed 245 °C at any time.

Dry Pack Information

The products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the products must be baked according to J-STD-033.

Surface Mount Assembly and Repair

Assembly

This product is **not** recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the product during the second reflow process.

Repair

For a successful repair (removal and replacement) of a LGA product, a dedicated rework system should be used. The rework system should preferably utilize a reflow station and a bottom side heater might also be needed for the operation.

TECHNICAL REFERENCE DOCUMENT: SAFETY

Safety specifications

Flex Power Modules' DC/DC converters and DC/DC regulators are designed in accordance with the safety standards *IEC 62368-1*, *EN 62368-1* and *UL 62368-1 Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power Interface Modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "conditions of acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (please refer to *Technical Specification under Mechanical Information* for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use shall comply with the requirements in *IEC/EN/UL 62368-1*. Product related standards, e.g. *IEEE 802.3af Power over Ethernet*, and *ETS-300132-2 Power interface at the input to telecom equipment, operated by direct current (dc)* are based on *IEC/EN/UL 62368-1* with regards to safety.

All Flex Power Modules' DC/DC converters, Power Interface Modules and DC/DC regulators are recognized and certified in accordance with *IEC/EN/UL 62368-1*. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to *IEC 62368-1 1-10 Fire hazard testing, test flames – 50 W horizontal and vertical flame test methods*.

Non-isolated DC/DC regulators

The DC/DC regulator output is ES1 energy source if the input source meets the requirements for ES1 according to *IEC/EN/UL 62368-1*.