



Vertical SIP



Horizontal SMD



## Key features

- High efficiency up to 96.2% at 12 V<sub>in</sub>, 5 V<sub>out</sub> full load.
- Paralleling up to 4 units (160A)
- Remote control
- Power Good
- Synchronization and phase spreading
- Excellent thermal performance
- Configuration and monitoring via PMBus

## Soldering methods

- Wave soldering (SIP)
- Reflow (SIP and SMD)

## BMR473

### 40A digital PoL regulator

The BMR473 is a digital PoL regulator available in a horizontal surface mount or vertical SIP package for board space optimization.

The product is rated at 40A continuous and up to 4 modules can be paralleled for up to 160A output current.

The BMR473 is a single-phase converter with high power density and efficiency levels are up to 96.2% at full load.

Input is rated from 6 to 15V and the output is programmable from 0.6 to 5V.

The BMR473 is designed for telecom and datacom applications but can also be applied in other areas such as industrial and transportation.

## Key electrical information

Parameter	Values
Input voltage range	6 - 15 V
Output voltage range	0.6 - 5 V
Max output current	40 A

## Mechanical

26.3 x 8.8 x 15.6 mm / 1.035 x 0.346 x 0.614 in (Vertical SIP)

19.0 x 13.0 x 7.5 mm / 0.748 x 0.512 x 0.296 in (Horizontal SMD)

## Application areas

- Telecom
- Datacom

## Product options

The table below describes the different product options.

For more information, please refer to Part 2 [Mechanical information](#).

Example: BMR473 2 0 01 /001						B	Definitions
<b>Product family</b>	BMR473						
<b>Mounting options</b>		2					1 = Surface mount 2 = Single in line package (SIP)
<b>Pin length options</b>			0				0 = standard (4.57 mm, SIP) 1 = short pin option (3.69 mm, SIP) 2 = long pin option (5.33 mm)  0 = solder bump (SMD)
<b>Other hardware variants</b>				01			01 = standard
<b>Configuration code</b>					/001		/001 = standard config. (positive remote control)
<b>Packaging options</b>						B	B = tray (one full package with 240 pieces) C = Tape and reel (one full package with 200 pieces)

If you do not find the variant you are looking for, please contact us at [Flex Power Modules](#).

## Order number examples

Part number	V <sub>in</sub>	outputs	configuration
BMR4732001/001	6 – 15 V	0.6 – 5 V, 40 A/100W	SIP 4.57 mm pins / positive logic / dry pack, tray
BMR4731001/001	6 – 15 V	0.6 – 5 V, 40 A/100W	SMD solder bump/ positive logic / dry pack, tape & reel

## Part 1: Electrical specifications

### Absolute maximum ratings

Stress in excess of our defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits*, are normally tested with one parameter at a time exceeding the limits in the electrical specification.

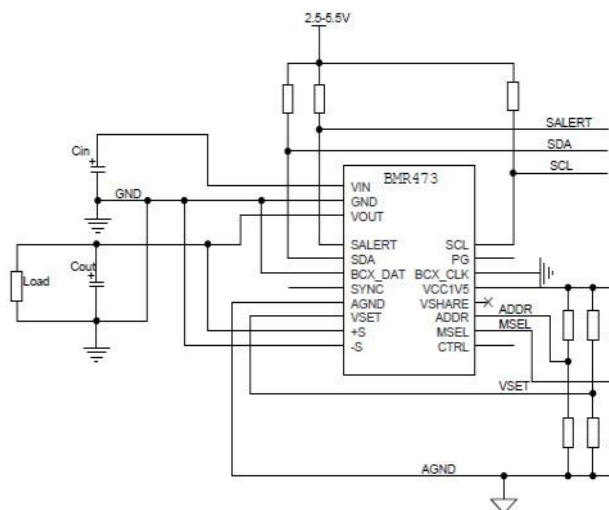
Characteristics		min	typ	max	Unit
Operating temperature (T <sub>PI</sub> )		-40		125	°C
Storage temperature		-40		125	°C
Input voltage (V <sub>in</sub> )		-0.3		16	V
Signal I/O voltage	SCL, SDA, SALERT, SYNC, BCX_DAT, BCX_CLK, CTRL, PG	-0.3		5.5	V
Ground voltage differential	-S, AGND, GND	-0.3		0.3	V
Analog pin voltage	V <sub>out</sub> , +S	-0.3		5.5	V
	ADDR, VSET, MSEL	-0.3		1.65	V

### Reliability

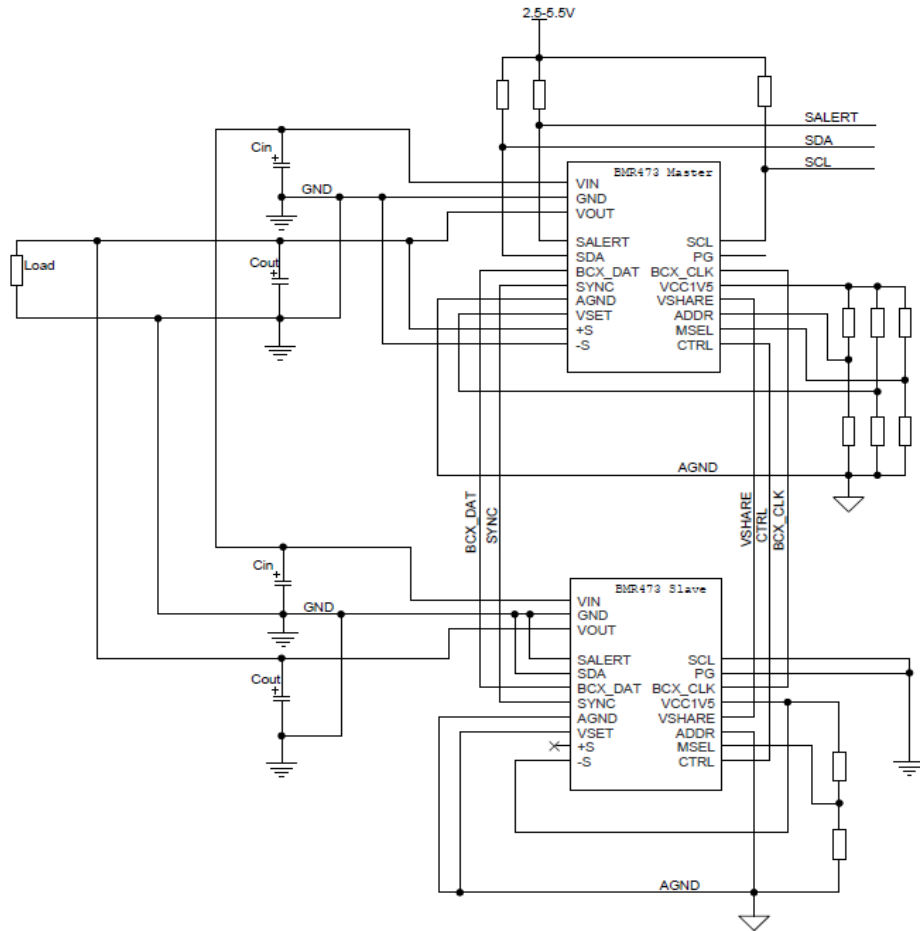
Failure rate ( $\lambda$ ) and mean time (50%) between failures (MTBF= 1/  $\lambda$ ) are calculated based on *Telcordia SR-332 Issue 4: Method 1, Case 3, (80% of I<sub>out</sub>, T<sub>PI</sub>=40°C, Airflow=200 LFM)*.

	Mean	90% confidence level	Unit
Steady-state failure rate ( $\lambda$ )	26	32	nfailures/h
Standard deviation ( $\sigma$ )	4.9		nfailures/h
MTBF	38.39	30.97	MHr

### Typical application diagram (Stand Alone)



Typical application diagram (2 modules paralleling)



**Electrical specifications for BMR4732001 (Vertical SIP)**

Min and Max values are valid for:  $T_{P1} = -40$  to  $+85^{\circ}\text{C}$ ,  $V_{in} = 6$  to  $15\text{ V}$ , unless otherwise specified under conditions. Typical values given at:  $T_{P1} = +25^{\circ}\text{C}$ ,  $V_{in} = 12\text{ V}$ , max  $I_{out}$ , unless otherwise specified under conditions.

Additional external  $C_{in} = 5 \times 22\ \mu\text{F}$  ceramic +  $470\ \mu\text{F}$  OSCON (ESR  $14\ \text{m}\Omega$ ),  $C_{out} = 5 \times 100\ \mu\text{F}$  ceramic +  $4 \times 470\ \mu\text{F}$  POSCAP (ESR  $10\ \text{m}\Omega$ ).

Characteristic	descriptions	conditions	min	typical	max	unit
<b>Input characteristics</b>						
Input voltage range ( $V_{in}$ )		$0.6\text{ V} \leq V_{out} \leq 3.3\text{ V}$	6	12	15	V
		$3.3\text{ V} < V_{out} \leq 5.0\text{ V}$	7	12	15	V
Input idling power	$I_{out} = 0\text{ A}$	$V_{out} = 0.6\text{ V}$		0.7		W
		$V_{out} = 1.0\text{ V}$		0.7		W
		$V_{out} = 1.8\text{ V}$		1.0		W
		$V_{out} = 2.5\text{ V}$		1.4		W
		$V_{out} = 3.3\text{ V}$		1.7		W
		$V_{out} = 5.0\text{ V}$		2.5		W
Input standby power	Turned off with CTRL pin			0.2		W
Internal input capacitance				110		$\mu\text{F}$
Recommended external input ceramic capacitance, note 1			110			$\mu\text{F}$
Recommended external input bulk capacitance, note 1			470			$\mu\text{F}$
<b>Output characteristics</b>						
Output voltage	Default value			1.0		V
Output voltage adjust range			0.6		5.0	V
Output voltage adjust range including margining, note 8			0.57		5.25	V
Output voltage set-point resolution		$0.6\text{ V} \leq V_{out} \leq 1.2\text{ V}$		10		mV
		$1.2\text{ V} \leq V_{out} \leq 2.4\text{ V}$		20		mV
		$2.4\text{ V} \leq V_{out} \leq 5.0\text{ V}$		40		mV
Output voltage accuracy	Including line, load and temperature		-1		1	% $V_o$

## Electrical specifications for BMR4732001 (Vertical SIP)

Characteristic	descriptions	conditions	min	typical	max	unit
Output line regulation	$I_{out} = \text{max } I_{out}$	$V_{out} = 0.6 \text{ V}$		1		mV
		$V_{out} = 1.0 \text{ V}$		2		
		$V_{out} = 1.8 \text{ V}$		2		
		$V_{out} = 2.5 \text{ V}$		2		
		$V_{out} = 3.3 \text{ V}$		2		
		$V_{out} = 5.0 \text{ V}$		4		
Output load regulation	$I_{out} = 0\text{-}100\%$	$V_{out} = 0.6 \text{ V}$		1		mV
		$V_{out} = 1.0 \text{ V}$		1		
		$V_{out} = 1.8 \text{ V}$		1		
		$V_{out} = 2.5 \text{ V}$		1		
		$V_{out} = 3.3 \text{ V}$		1		
		$V_{out} = 5.0 \text{ V}$		2		
Output ripple & noise, note 2	Up to 20 MHz bandwidth	$V_{out} = 0.6 \text{ V}$		6		mVp-p
		$V_{out} = 1.0 \text{ V}$		8		
		$V_{out} = 1.8 \text{ V}$		11		
		$V_{out} = 2.5 \text{ V}$		12		
		$V_{out} = 3.3 \text{ V}$		12		
		$V_{out} = 5.0 \text{ V}$		10		
Load transient voltage deviation, Load step 25-75-25% of max $I_o$ , note 3	$di/dt=2 \text{ A}/\mu\text{s}$ , $C_{out} = 5 \times 100 \mu\text{F}$ ceramic + 4 x 470 $\mu\text{F}$ POSCAP (ESR 10 m $\Omega$ )	$V_{out} = 0.6 \text{ V}$		110		mV
		$V_{out} = 1.0 \text{ V}$		110		
		$V_{out} = 1.8 \text{ V}$		210		
		$V_{out} = 2.5 \text{ V}$		270		
		$V_{out} = 3.3 \text{ V}$		270		
		$V_{out} = 5.0 \text{ V}$		180		
Load transient recovery time, Load step 25-75-25% of max $I_o$ , note 3	$di/dt=2 \text{ A}/\mu\text{s}$ , $C_{out} = 5 \times 100 \mu\text{F}$ ceramic + 4 x 470 $\mu\text{F}$ POSCAP (ESR 10 m $\Omega$ )	$V_{out} = 0.6 \text{ V}$		400		$\mu\text{s}$
		$V_{out} = 1.0 \text{ V}$		400		
		$V_{out} = 1.8 \text{ V}$		400		
		$V_{out} = 2.5 \text{ V}$		400		
		$V_{out} = 3.3 \text{ V}$		400		
		$V_{out} = 5.0 \text{ V}$		400		

## Electrical specifications for BMR4732001 (Vertical SIP)

Characteristic	descriptions	conditions	min	typical	max	unit
Output current		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$	0		40	A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$	0		30	A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$	0		20	A
Output current limit		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$		52		A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$		39		A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$		26		A
Short circuit current	Hiccup mode, RMS value	$V_{\text{out}} = 0.6\text{ V}$		9.3		A
		$V_{\text{out}} = 1.0\text{ V}$		7.4		A
		$V_{\text{out}} = 1.8\text{ V}$		6.4		A
		$V_{\text{out}} = 2.5\text{ V}$		3.3		A
		$V_{\text{out}} = 3.3\text{ V}$		3.2		A
		$V_{\text{out}} = 5.0\text{ V}$		1.6		A
Efficiency ( $\eta$ )	50% of max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		85.4		%
		$V_{\text{out}} = 1.0\text{ V}$		89.9		%
		$V_{\text{out}} = 1.8\text{ V}$		93.0		%
		$V_{\text{out}} = 2.5\text{ V}$		94.0		%
		$V_{\text{out}} = 3.3\text{ V}$		94.7		%
		$V_{\text{out}} = 5.0\text{ V}$		94.6		%
	100% of max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		81.0		%
		$V_{\text{out}} = 1.0\text{ V}$		86.6		%
		$V_{\text{out}} = 1.8\text{ V}$		90.7		%
		$V_{\text{out}} = 2.5\text{ V}$		93.4		%
		$V_{\text{out}} = 3.3\text{ V}$		94.2		%
		$V_{\text{out}} = 5.0\text{ V}$		95.6		%
Power dissipation	at max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		5.7	8.5	W
		$V_{\text{out}} = 1.0\text{ V}$		6.2	9	W
		$V_{\text{out}} = 1.8\text{ V}$		7.4	10	W
		$V_{\text{out}} = 2.5\text{ V}$		5.3	8	W
		$V_{\text{out}} = 3.3\text{ V}$		6.1	8	W
		$V_{\text{out}} = 5.0\text{ V}$		4.6	7	W
Internal output capacitance				350		$\mu\text{F}$
Recommended external output ceramic capacitance, note 4		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	200	500		$\mu\text{F}$
Recommended external output bulk capacitance, note 4		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	470	1880	10000	$\mu\text{F}$

**Electrical specifications for BMR4731001 (Horizontal SMD)**

Min and Max values are valid for:  $T_{P1} = -40$  to  $+85^{\circ}\text{C}$ ,  $V_{in} = 6$  to  $15$  V, unless otherwise specified under conditions. Typical values given at:  $T_{P1} = +25^{\circ}\text{C}$ ,  $V_{in} = 12$  V, max  $I_{out}$ , unless otherwise specified under conditions.

Additional external  $C_{in} = 8 \times 22 \mu\text{F}$  ceramic +  $470 \mu\text{F}$  OSCON (ESR  $14 \text{ m}\Omega$ ),  $C_{out} = 8 \times 100 \mu\text{F}$  ceramic +  $4 \times 470 \mu\text{F}$  POSCAP (ERS  $10 \text{ m}\Omega$ ).

Characteristic	descriptions	conditions	min	typical	max	unit
<b>Input characteristics</b>						
Input voltage range ( $V_{in}$ )		$0.6 \text{ V} \leq V_{out} \leq 3.3 \text{ V}$	6	12	15	V
		$3.3 \text{ V} < V_{out} \leq 5.0 \text{ V}$	7	12	15	V
Input idling power	$I_{out} = 0 \text{ A}$	$V_{out} = 0.6 \text{ V}$		0.7		W
		$V_{out} = 1.0 \text{ V}$		0.7		W
		$V_{out} = 1.8 \text{ V}$		1.0		W
		$V_{out} = 2.5 \text{ V}$		1.4		W
		$V_{out} = 3.3 \text{ V}$		1.5		W
		$V_{out} = 5.0 \text{ V}$		2.0		W
Input standby power	Turned off with CTRL pin			0.2		W
Internal input capacitance				68		$\mu\text{F}$
Recommended external input ceramic capacitance, note 1			176			$\mu\text{F}$
Recommended external input bulk capacitance, note 1			470			$\mu\text{F}$
<b>Output characteristics</b>						
Output voltage	Default value			1.0		V
Output voltage adjust range			0.6		5.0	V
Output voltage adjust range including margining, Note 8			0.57		5.25	V
Output voltage set-point resolution		$0.6 \text{ V} \leq V_{out} \leq 1.2 \text{ V}$		10		mV
		$1.2 \text{ V} \leq V_{out} \leq 2.4 \text{ V}$		20		mV
		$2.4 \text{ V} \leq V_{out} \leq 5.0 \text{ V}$		40		mV
Output voltage accuracy	Including line, load and temperature		-1		1	% $V_o$

## Electrical specifications for BMR4731001 (Horizontal SMD)

Characteristic	descriptions	conditions	min	typical	max	unit
Output line regulation	$I_{out} = \text{max } I_{out}$	$V_{out} = 0.6 \text{ V}$		1		mV
		$V_{out} = 1.0 \text{ V}$		1		
		$V_{out} = 1.8 \text{ V}$		1		
		$V_{out} = 2.5 \text{ V}$		1		
		$V_{out} = 3.3 \text{ V}$		1		
		$V_{out} = 5.0 \text{ V}$		1		
Output load regulation	$I_{out} = 0\text{-}100\%$	$V_{out} = 0.6 \text{ V}$		1		mV
		$V_{out} = 1.0 \text{ V}$		1		
		$V_{out} = 1.8 \text{ V}$		1		
		$V_{out} = 2.5 \text{ V}$		1		
		$V_{out} = 3.3 \text{ V}$		1		
		$V_{out} = 5.0 \text{ V}$		1		
Output ripple & noise, note 2	Up to 20 MHz bandwidth	$V_{out} = 0.6 \text{ V}$		4		mVp-p
		$V_{out} = 1.0 \text{ V}$		5		
		$V_{out} = 1.8 \text{ V}$		8		
		$V_{out} = 2.5 \text{ V}$		10		
		$V_{out} = 3.3 \text{ V}$		12		
		$V_{out} = 5.0 \text{ V}$		15		
Load transient voltage deviation, Load step 25-75-25% of max $I_o$ , note 3	$di/dt=2 \text{ A}/\mu\text{s}$ , $C_{out} = 8 \times 100 \mu\text{F}$ ceramic + 4 x 470 $\mu\text{F}$ POSCAP (ESR 10 m $\Omega$ )	$V_{out} = 0.6 \text{ V}$		110		mV
		$V_{out} = 1.0 \text{ V}$		110		
		$V_{out} = 1.8 \text{ V}$		200		
		$V_{out} = 2.5 \text{ V}$		260		
		$V_{out} = 3.3 \text{ V}$		260		
		$V_{out} = 5.0 \text{ V}$		180		
Load transient recovery time, Load step 25-75-25% of max $I_o$ , note 3	$di/dt=2 \text{ A}/\mu\text{s}$ , $C_{out} = 8 \times 100 \mu\text{F}$ ceramic + 4 x 470 $\mu\text{F}$ POSCAP (ESR 10 m $\Omega$ )	$V_{out} = 0.6 \text{ V}$		400		$\mu\text{s}$
		$V_{out} = 1.0 \text{ V}$		400		
		$V_{out} = 1.8 \text{ V}$		400		
		$V_{out} = 2.5 \text{ V}$		400		
		$V_{out} = 3.3 \text{ V}$		400		
		$V_{out} = 5.0 \text{ V}$		400		

## Electrical specifications for BMR4731001 (Horizontal SMD)

Characteristic	descriptions	conditions	min	typical	max	unit
Output current		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$	0		40	A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$	0		30	A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$	0		20	A
Output current limit		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$		52		A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$		39		A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$		26		A
Short circuit current	Hiccup mode, RMS value	$V_{\text{out}} = 0.6\text{ V}$		9.3		A
		$V_{\text{out}} = 1.0\text{ V}$		7.4		A
		$V_{\text{out}} = 1.8\text{ V}$		6.4		A
		$V_{\text{out}} = 2.5\text{ V}$		3.3		A
		$V_{\text{out}} = 3.3\text{ V}$		3.2		A
		$V_{\text{out}} = 5.0\text{ V}$		1.6		A
Efficiency ( $\eta$ )	50% of max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		86.3		%
		$V_{\text{out}} = 1.0\text{ V}$		90.5		%
		$V_{\text{out}} = 1.8\text{ V}$		93.5		%
		$V_{\text{out}} = 2.5\text{ V}$		94.4		%
		$V_{\text{out}} = 3.3\text{ V}$		95.2		%
		$V_{\text{out}} = 5.0\text{ V}$		95.5		%
	100% of max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		82.6		%
		$V_{\text{out}} = 1.0\text{ V}$		87.8		%
		$V_{\text{out}} = 1.8\text{ V}$		91.7		%
		$V_{\text{out}} = 2.5\text{ V}$		94.0		%
		$V_{\text{out}} = 3.3\text{ V}$		95.0		%
		$V_{\text{out}} = 5.0\text{ V}$		96.2		%
Power dissipation	at max $I_{\text{out}}$	$V_{\text{out}} = 0.6\text{ V}$		5.1	8.5	W
		$V_{\text{out}} = 1.0\text{ V}$		5.6	9	W
		$V_{\text{out}} = 1.8\text{ V}$		6.5	10	W
		$V_{\text{out}} = 2.5\text{ V}$		4.8	8	W
		$V_{\text{out}} = 3.3\text{ V}$		5.3	8	W
		$V_{\text{out}} = 5.0\text{ V}$		4.0	7	W
Internal output capacitance				72		$\mu\text{F}$
Recommended external output ceramic capacitance, note 4		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	500	800		$\mu\text{F}$
Recommended external output bulk capacitance, note 4		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	470	1880	10000	$\mu\text{F}$

## Electrical specifications for BMR473

Characteristic	descriptions	conditions	min	typical	max	unit
<b>Protection characteristics</b>						
Input turn on voltage	Default value, Note 9	$0.6\text{ V} \leq V_{\text{out}} \leq 3.3\text{ V}$		5.5		V
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$		6.5		V
	PMBus configurable range		5.5		15	V
	Resolution			0.25		V
Input Under Voltage Lockout, UVLO	Default value, Note 10	$0.6\text{ V} \leq V_{\text{out}} \leq 3.3\text{ V}$		4.5		V
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$		5.5		V
	PMBus configurable range		4.5		15	V
	Resolution			0.25		V
Input Over Voltage Protection, IOVP	Default value			16		V
	PMBus configurable range		6		16	V
	Resolution			1		V
	Response delay			0		µs
	Fault response		Automatic restart, 70ms			
Output Over Voltage Protection, OVP	Default value			115		%
	PMBus configurable range		105		140	%
	Resolution			2.5		%
	Fault response		Automatic restart, 70ms			
Output Under Voltage Protection, UVP	Default value			85		%
	PMBus configurable range		60		95	%
	Resolution			2.5		%
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			
Over Current Protection, OCP	Default value, Note 11			52		A
	PMBus configurable range		8		52	A
	Resolution			2		A
	Response delay time		7 PWM cycles			
	Fault response		Automatic restart, 70ms			
Over Temperature Protection, OTP, note 5	Default value			135		°C
	PMBus configurable range		0		150	°C
	Resolution			1		°C
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			

## Electrical specifications for BMR473

Characteristic	descriptions	conditions	min	typical	max	unit
<b>Other characteristics</b>						
Switching frequency (f <sub>s</sub> )	Default value			450		kHz
	PMBus configurable range, note 6		450		900	kHz
	Set-point Accuracy		-10		10	%
Frequency synchronization, SYNC	SYNC output duty cycle			50		%
	SYNC input minimum pulse width				200	ns
	Allowable SYNC pin frequency difference from FREQUENCY_SWITCH frequency		-20		20	%
Initialization time				10		ms
Output voltage turn on delay time	Default value			10		ms
	PMBus configurable range (TON_DELAY)		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn on ramp up time (0-100% of V <sub>o</sub> )	Default value			10		ms
	PMBus configurable range (TON_RISE), note 7		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Output voltage turn off delay time	Default value			0		ms
	PMBus configurable range (TOFF_DELAY), note 7		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn off fall time (100-0% of V <sub>o</sub> )	Default value		Disabled, turn off immediately upon expiration of Turn off delay			
	PMBus configurable range (TOFF_FALL)		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Power Good, PG	PG assertion threshold on V <sub>o</sub> rising			95		% V <sub>o</sub>
	PG de-assertion threshold on V <sub>o</sub> falling			95		% V <sub>o</sub>

## Electrical specifications for BMR473

Characteristic	descriptions	conditions	min	typical	max	unit
Monitoring accuracy	Input voltage, READ_VIN		-3		3	%
	Output voltage, READ_VOUT		-2		2	%
	Output current, READ_IOUT		-5		5	A
	Temperature, READ_TEMPERATURE1		-3		3	°C
Logic output low level	SCL, SDA, SALERT, SYNC, PG, BCX_DAT, BCX_CLK				0.4	V
Logic output high level		2.25				V
Logic input low level	SCL, SDA, SYNC, CTRL				0.8	V
Logic input high level		1.35				V
Logic pin internal capacitance	PG			100		pF
Logic pin internal pull up resistance	PG to 5V, CTRL to 5V			10		kΩ
Supported PMBus operating frequency range			10		1000	kHz
SMBus Bus free time			0.5			μs
SMBus SDA setup time from SCL			0.26			μs
SMBus SDA hold time from SCL			0			μs
SMBus START/STOP condition setup/hold time			0.26			μs
SCL low period			0.5			μs
SCL high period			0.26			μs

Note 1: See section "Input capacitors" in "Design & Application Guide".

Note 2: See graph "Output ripple and noise".

Note 3: See graph "Transient response".

Note 4: See section "Output capacitors" in "Design & Application Guide".

Note 5: Temperature of T<sub>p1</sub>, see section "Definition of product operating temperature".

Note 6: Effective switching frequency listed in section "Switching frequency" in "Design & Application Guide".

Note 7: Values less than 0.5 ms are supported as 0.5 ms.

Note 8: Should not exceed maximum output power 100 W.

Note 9: Change input turn on voltage to 6.5V when V<sub>out</sub>>3.3 V.

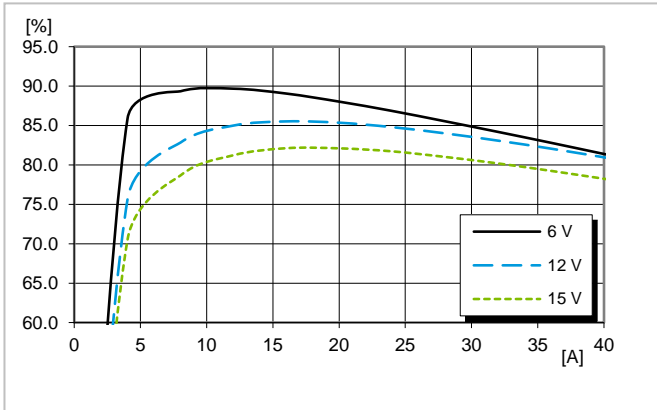
Note 10: Change UVLO to 5.5 V when V<sub>out</sub>>3.3 V.

Note 11: Decrease OCP when V<sub>out</sub>>1.8 V.

**Electrical graphs for BMR4732001 (Vertical SIP)**

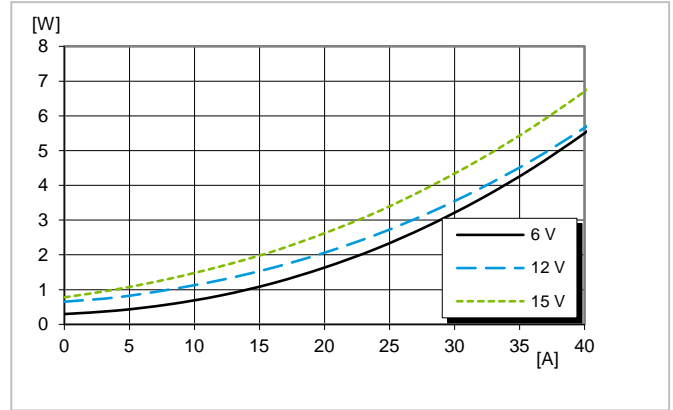
**V<sub>out</sub> = 0.6 V**

**Efficiency**



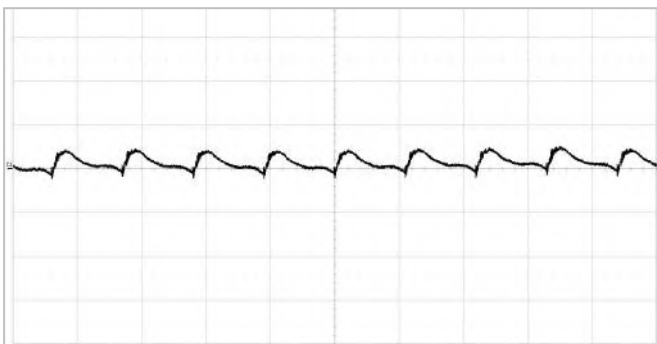
Efficiency vs. output current at T<sub>P1</sub> = +25°C

**Power dissipation**



Dissipated power vs. load current at T<sub>P1</sub> = +25°C

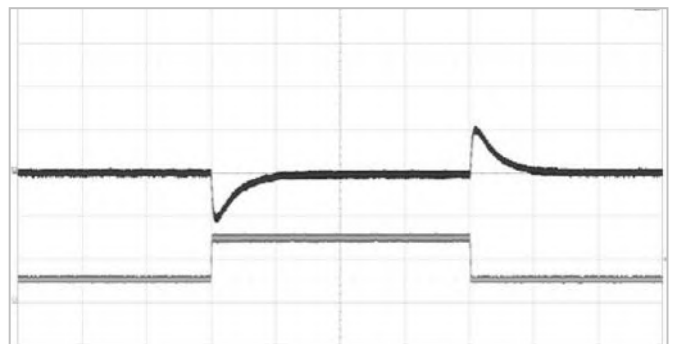
**Output ripple and noise**



Output voltage ripple at V<sub>I</sub>=12V, I<sub>o</sub>=max I<sub>o</sub>, T<sub>P1</sub> = +25°C

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth

**Transient response**



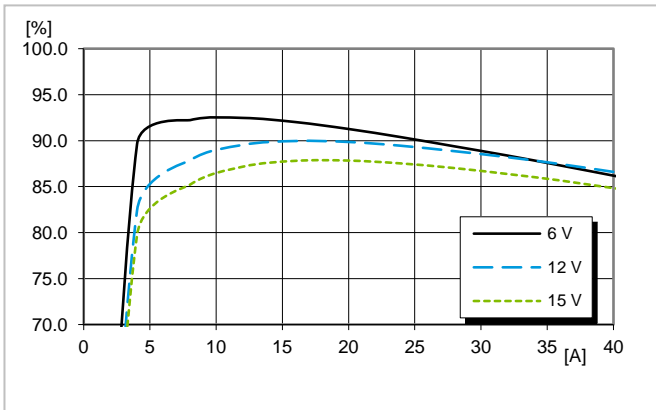
Output voltage response to output current change (10-30-10 A) at V<sub>I</sub>=12V, C<sub>O</sub>=5 x 100 μF ceramic + 4 x 470 μF POSCAP (ESR 10 mΩ), T<sub>P1</sub> = +25°C, di/dt=2A/μs.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

### Electrical graphs for BMR4732001 (Vertical SIP)

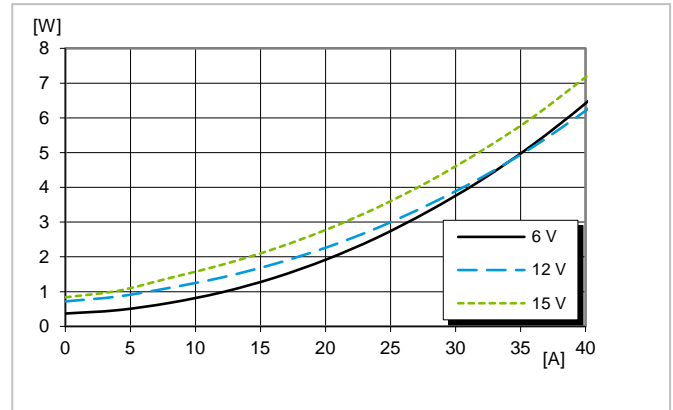
$V_{out} = 1.0\text{ V}$

#### Efficiency



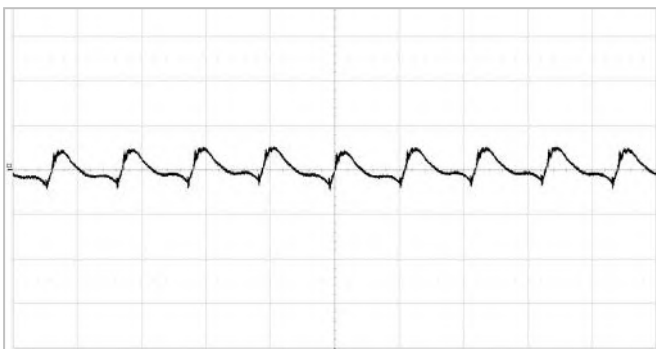
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

#### Power dissipation



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

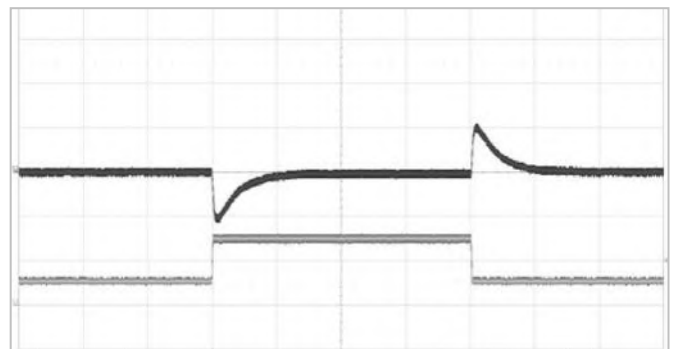
#### Output ripple and noise



Output voltage ripple at  $V_i=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2  $\mu\text{s}/\text{div}$ , 20 MHz bandwidth

#### Transient response



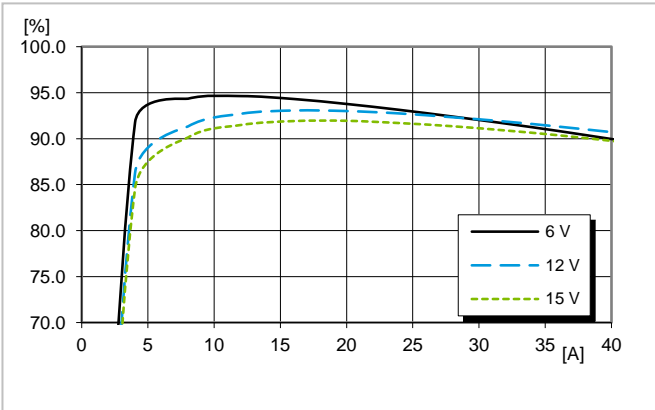
Output voltage response to output current change (10-30-10 A) at  $V_i=12\text{V}$ ,  $C_o=5 \times 100\ \mu\text{F}$  ceramic +  $4 \times 470\ \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}/\text{div}$

**Electrical graphs for BMR4732001 (Vertical SIP)**

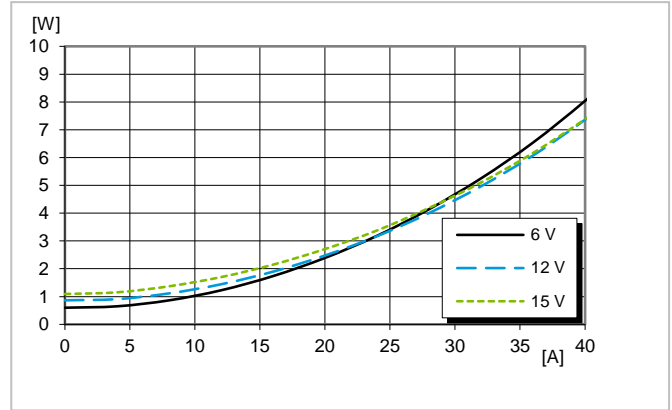
**V<sub>out</sub> = 1.8 V**

**Efficiency**



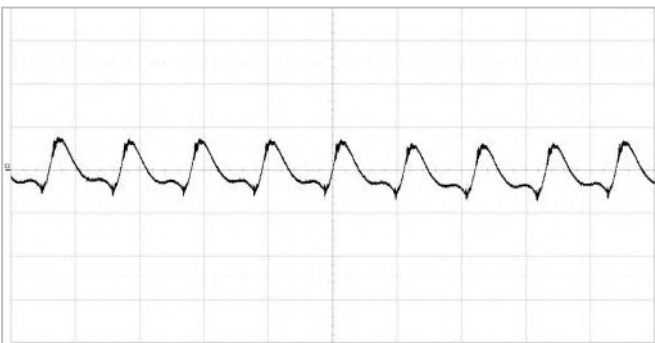
Efficiency vs. output power and input voltage at T<sub>P1</sub> = +25°C

**Power dissipation**



Dissipated power vs. load power at T<sub>P1</sub> = +25°C

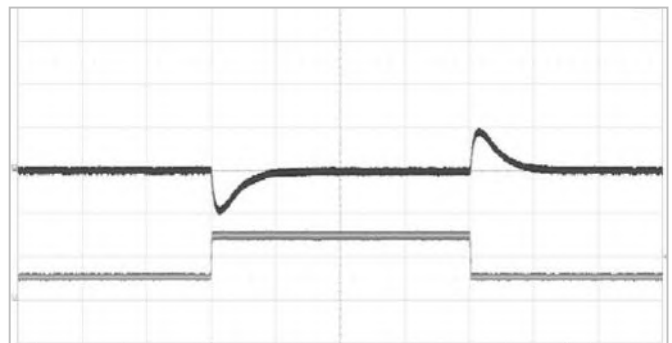
**Output ripple and noise**



Output voltage ripple at V<sub>I</sub>=12V, I<sub>o</sub>=max I<sub>o</sub>, T<sub>P1</sub> = +25°C

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth

**Transient response**



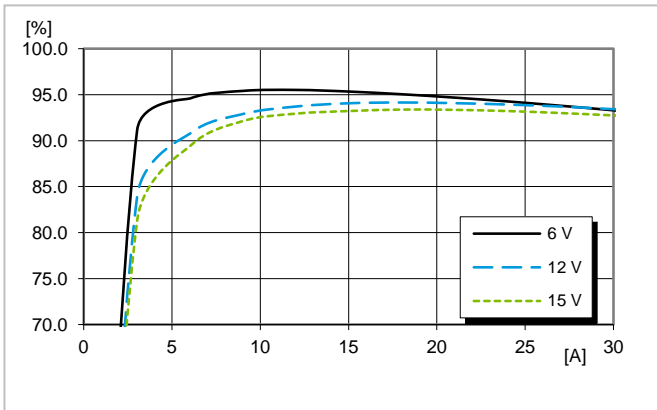
Output voltage response to output current change (10-30-10 A) at V<sub>I</sub>=12V, C<sub>O</sub>=5 x 100 μF ceramic + 4 x 470 μF POSCAP (ESR 10 mΩ), T<sub>P1</sub> = +25°C, di/dt=2A/μs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

**Electrical graphs for BMR4732001 (Vertical SIP)**

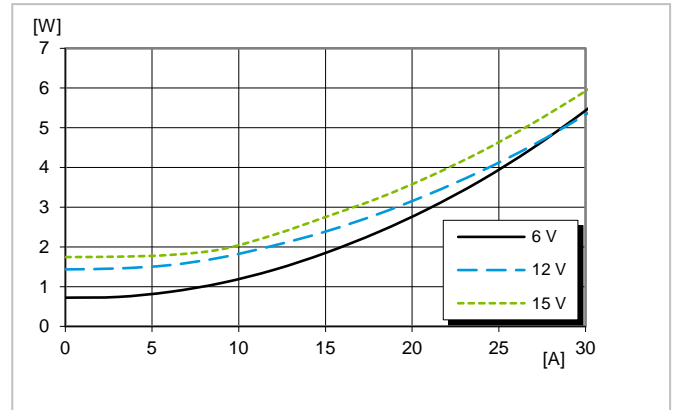
**V<sub>out</sub> = 2.5 V**

**Efficiency**



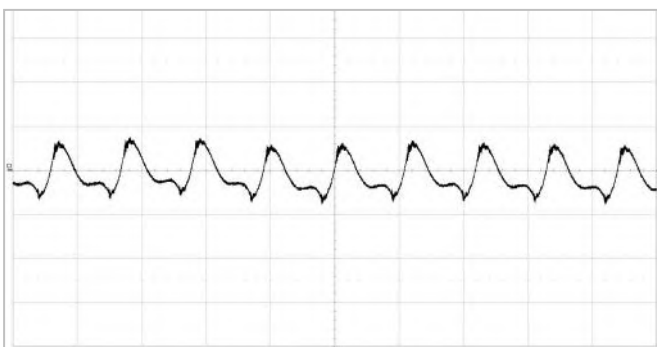
Efficiency vs. output power and input voltage at T<sub>P1</sub> = +25°C

**Power dissipation**



Dissipated power vs. load power at T<sub>P1</sub> = +25°C

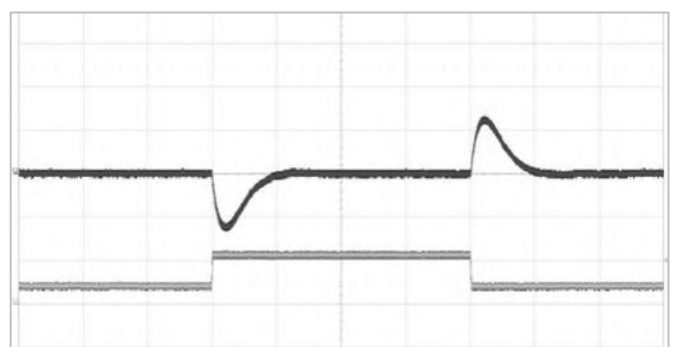
**Output ripple and noise**



Output voltage ripple at V<sub>I</sub>=12V, I<sub>o</sub>=max I<sub>o</sub>, T<sub>P1</sub> = +25°C

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth

**Transient response**



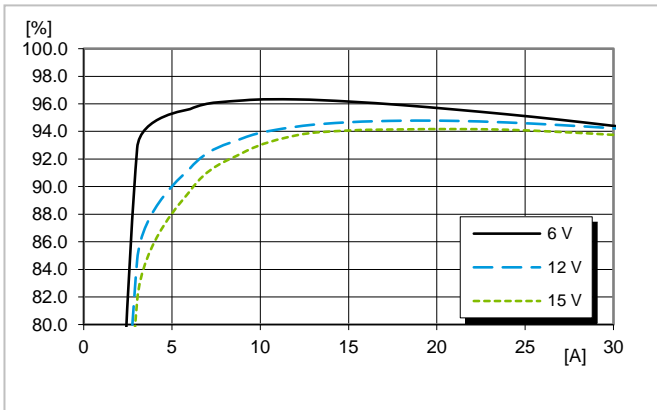
Output voltage response to output current change (7.5-22.5-7.5 A) at V<sub>I</sub>=12V, C<sub>O</sub>=5 x 100 μF ceramic + 4 x 470 μF POSCAP (ESR 10 mΩ), T<sub>P1</sub> = +25°C, di/dt=2A/μs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

**Electrical graphs for BMR4732001 (Vertical SIP)**

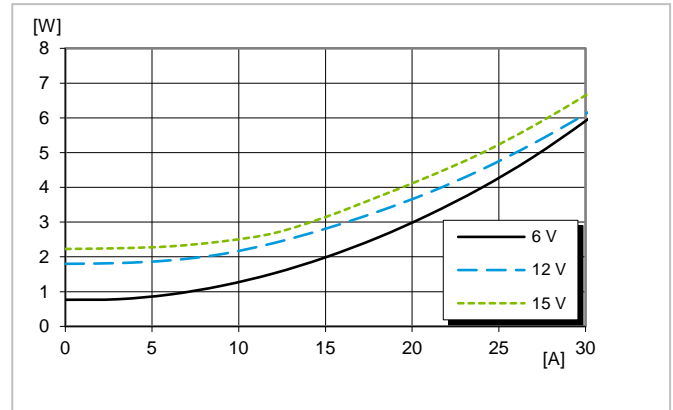
**V<sub>out</sub> = 3.3 V**

**Efficiency**



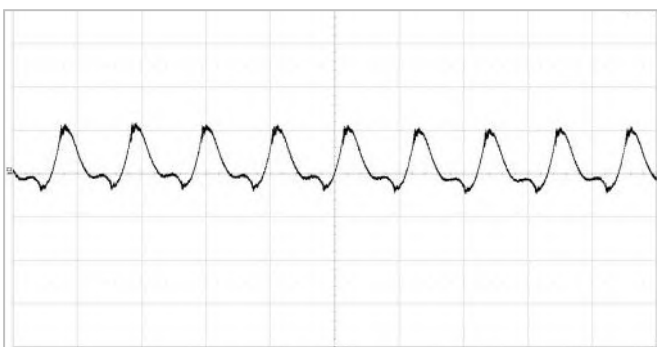
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

**Power dissipation**



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

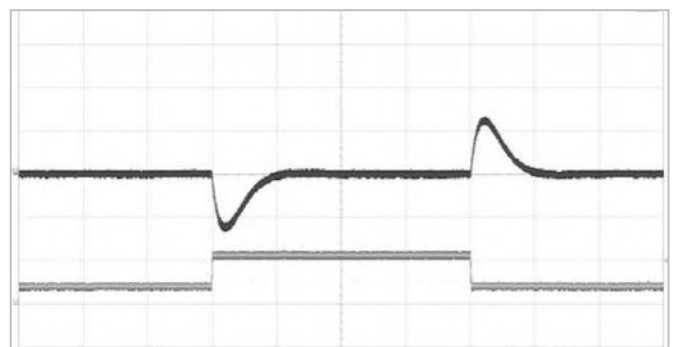
**Output ripple and noise**



Output voltage ripple at  $V_i=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2  $\mu\text{s}$ /div, 20 MHz bandwidth

**Transient response**



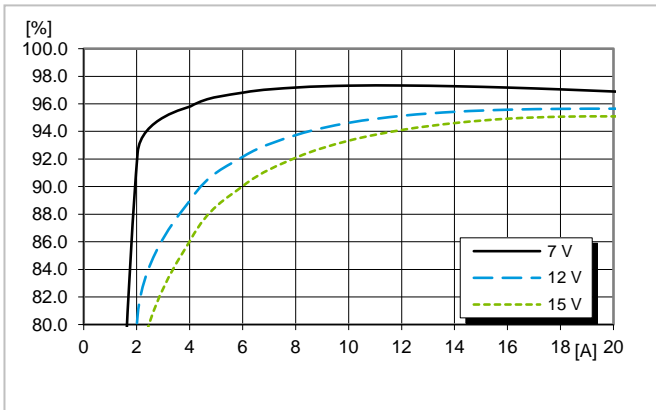
Output voltage response to output current change (7.5-22.5-7.5 A) at  $V_i=12\text{V}$ ,  $C_o=5 \times 100 \mu\text{F}$  ceramic +  $4 \times 470 \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}$ /div

**Electrical graphs for BMR4732001 (Vertical SIP)**

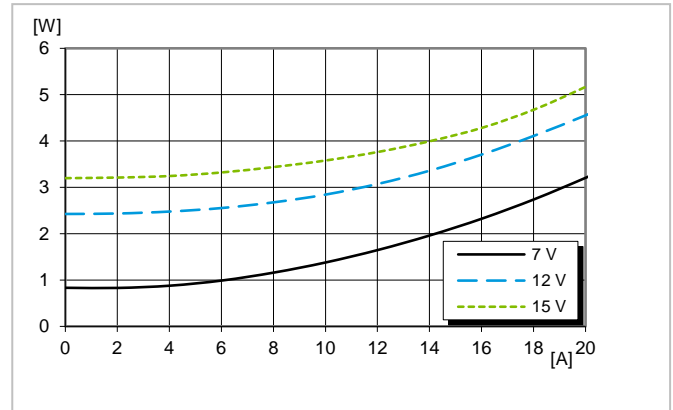
**V<sub>out</sub> = 5.0 V**

**Efficiency**



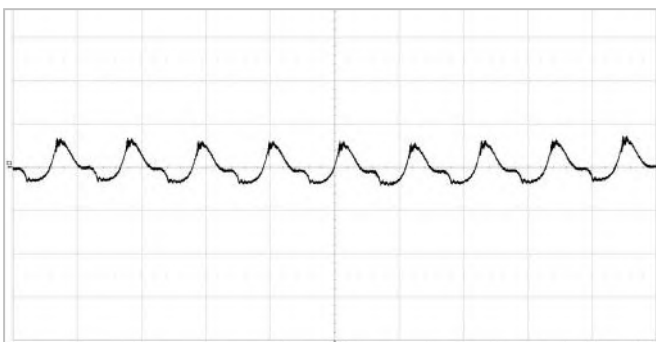
Efficiency vs. output power and input voltage at T<sub>P1</sub> = +25°C

**Power dissipation**



Dissipated power vs. load power at T<sub>P1</sub> = +25°C

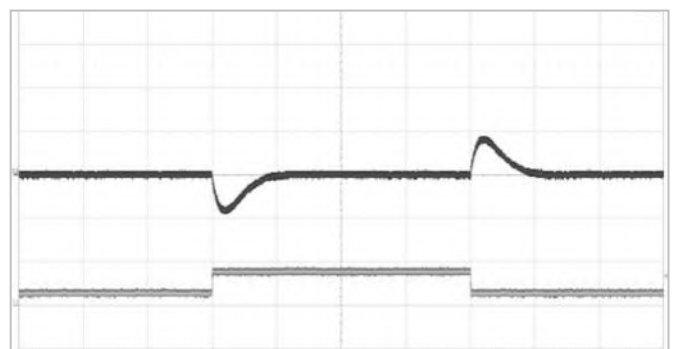
**Output ripple and noise**



Output voltage ripple at V<sub>I</sub>=12V, I<sub>o</sub>=max I<sub>o</sub>, T<sub>P1</sub> = +25°C

Scale: 5 mV/div, 2 μs/div, 20 MHz bandwidth

**Transient response**



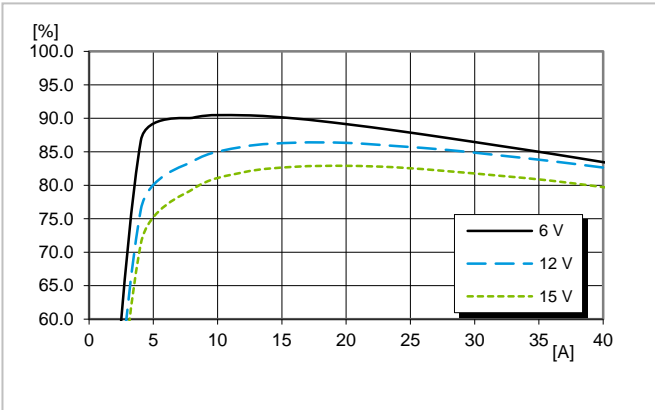
Output voltage response to output current change (5-15-5 A) at V<sub>I</sub>=12V, C<sub>o</sub>=5 x 100 μF ceramic + 4 x 470 μF POSCAP (ESR 10 mΩ), T<sub>P1</sub> = +25°C, di/dt=2A/μs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

**Electrical graphs for BMR4731001 (Horizontal SMD)**

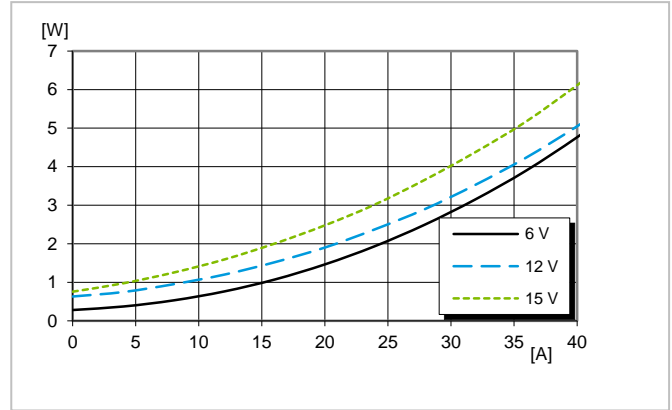
**V<sub>out</sub> = 0.6 V**

**Efficiency**



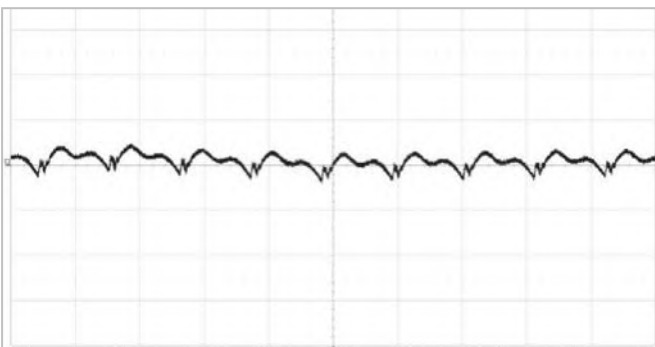
Efficiency vs. output current at  $T_{P1} = +25^{\circ}\text{C}$

**Power dissipation**



Dissipated power vs. load current at  $T_{P1} = +25^{\circ}\text{C}$

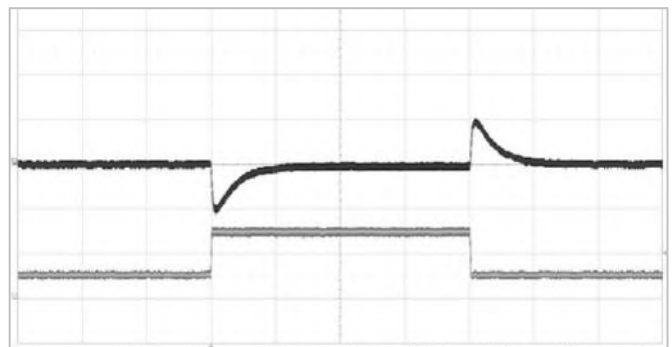
**Output ripple and noise**



Output voltage ripple at  $V_i=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2  $\mu\text{s}$ /div, 20 MHz bandwidth

**Transient response**



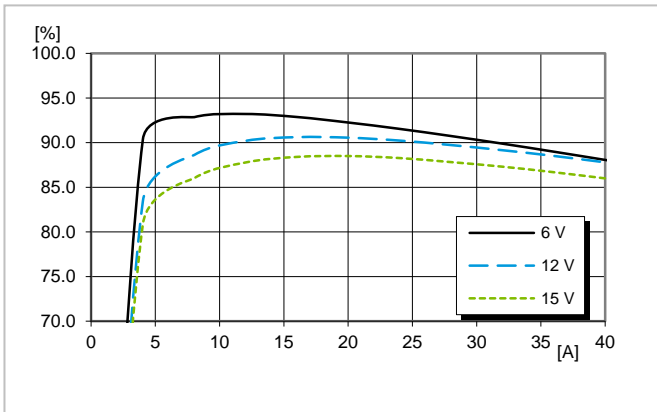
Output voltage response to output current change (10-30-10 A) at  $V_i=12\text{V}$ ,  $C_o=8 \times 100 \mu\text{F}$  ceramic + 4 x 470  $\mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}$ /div

### Electrical graphs for BMR4731001 (Horizontal SMD)

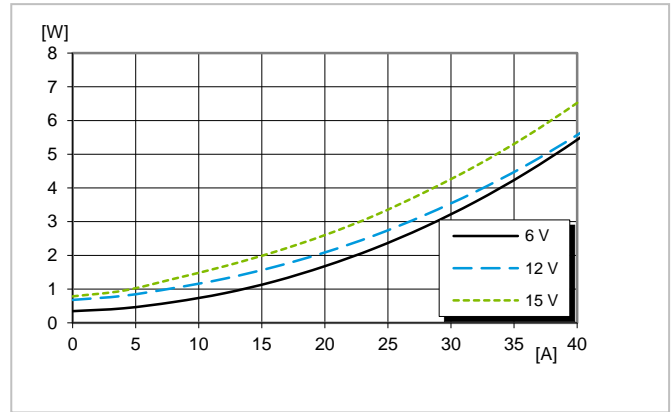
$V_{out} = 1.0\text{ V}$

#### Efficiency



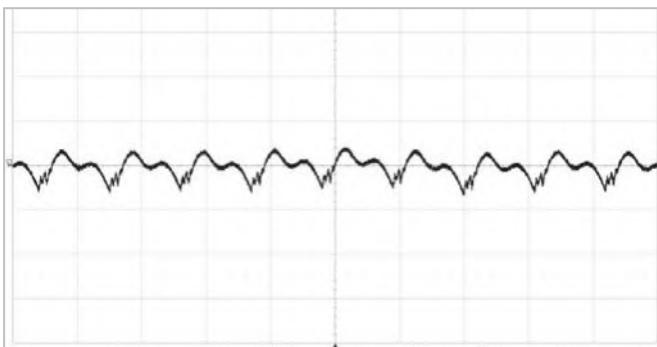
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

#### Power dissipation



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

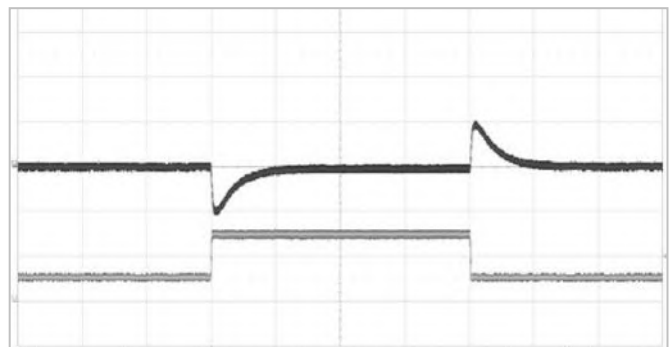
#### Output ripple and noise



Output voltage ripple at  $V_i=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2  $\mu\text{s}$ /div, 20 MHz bandwidth

#### Transient response



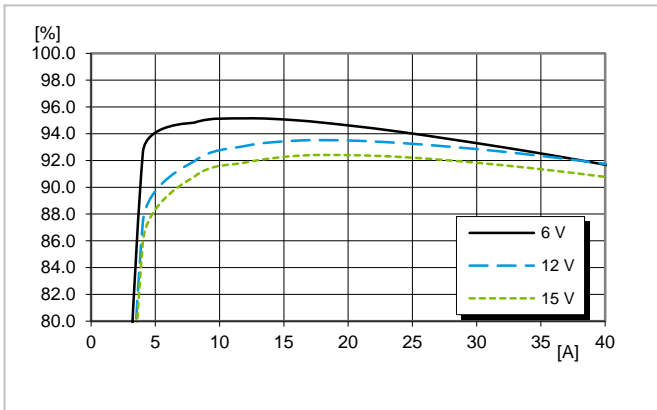
Output voltage response to output current change (10-30-10 A) at  $V_i=12\text{V}$ ,  $C_o=8 \times 100\ \mu\text{F}$  ceramic +  $4 \times 470\ \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}$ /div

### Electrical graphs for BMR4731001 (Horizontal SMD)

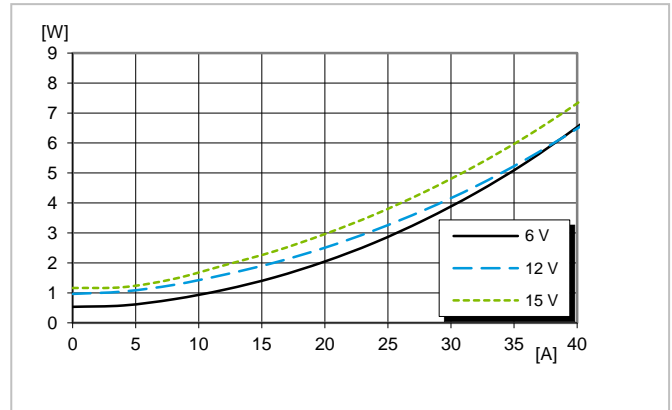
$V_{out} = 1.8\text{ V}$

#### Efficiency



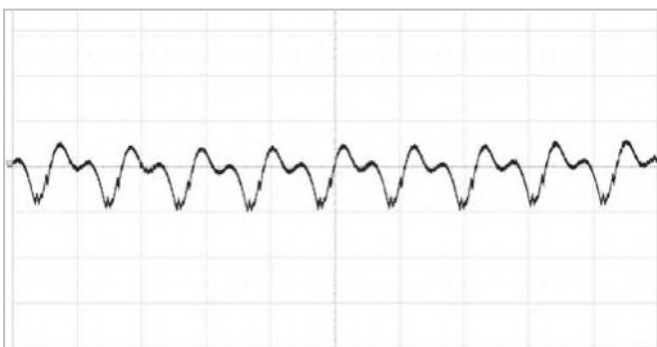
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

#### Power dissipation



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

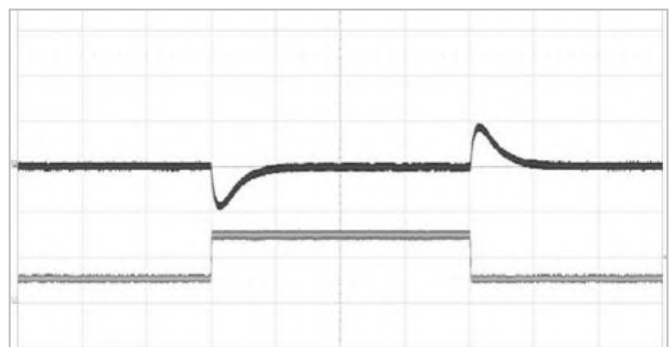
#### Output ripple and noise



Output voltage ripple at  $V_i=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2  $\mu\text{s}$ /div, 20 MHz bandwidth

#### Transient response



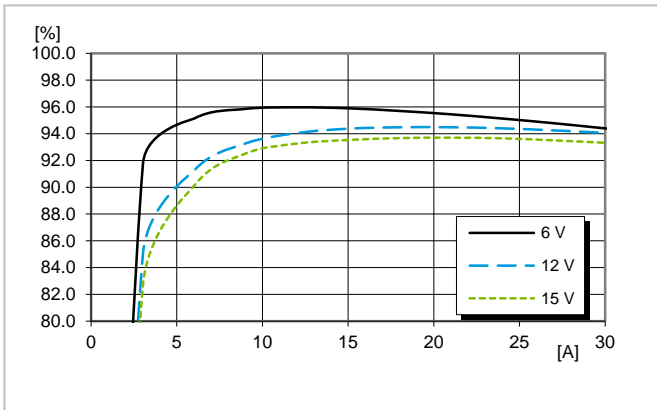
Output voltage response to output current change (10-30-10 A) at  $V_i=12\text{V}$ ,  $C_o=8 \times 100\ \mu\text{F}$  ceramic +  $4 \times 470\ \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}$ /div

Electrical graphs for BMR4731001 (Horizontal SMD)

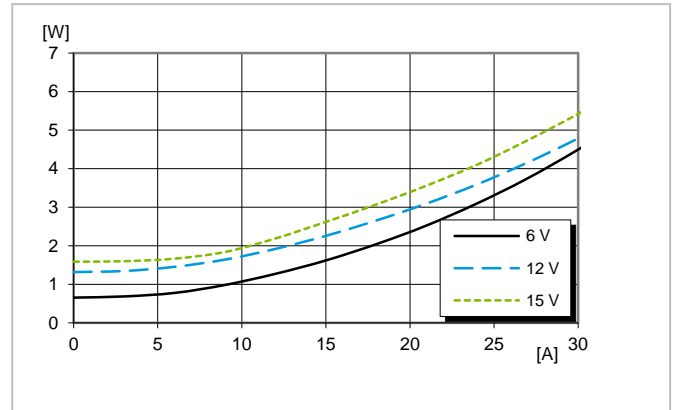
$V_{out} = 2.5 V$

Efficiency



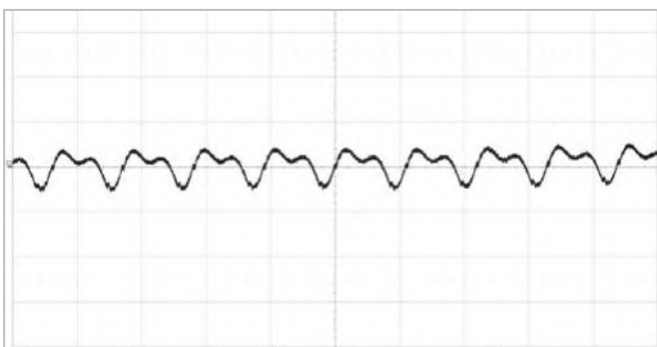
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}C$

Power dissipation



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}C$

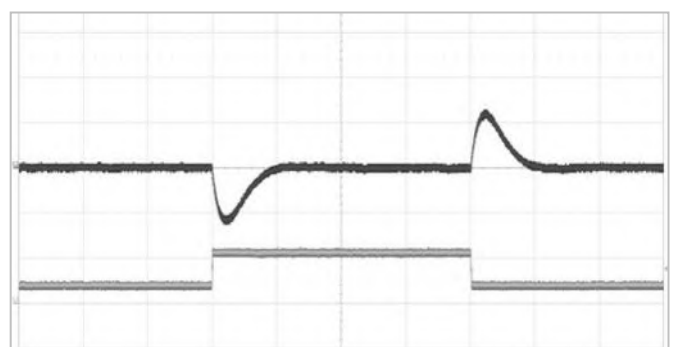
Output ripple and noise



Output voltage ripple at  $V_I=12V$ ,  $I_o=\max I_o$ ,  $T_{P1} = +25^{\circ}C$

Scale: 10 mV/div, 2  $\mu s$ /div, 20 MHz bandwidth

Transient response



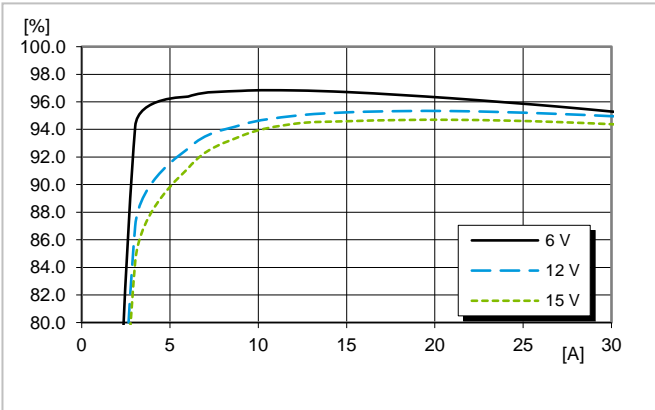
Output voltage response to output current change (7.5-22.5-7.5 A) at  $V_I=12V$ ,  $C_o=8 \times 100 \mu F$  ceramic +  $4 \times 470 \mu F$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}C$ ,  $di/dt=2A/\mu s$ .

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu s$ /div

**Electrical graphs for BMR4731001 (Horizontal SMD)**

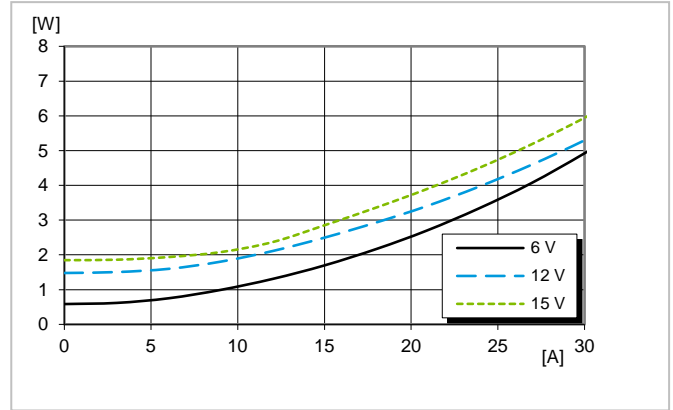
**V<sub>out</sub> = 3.3 V**

**Efficiency**



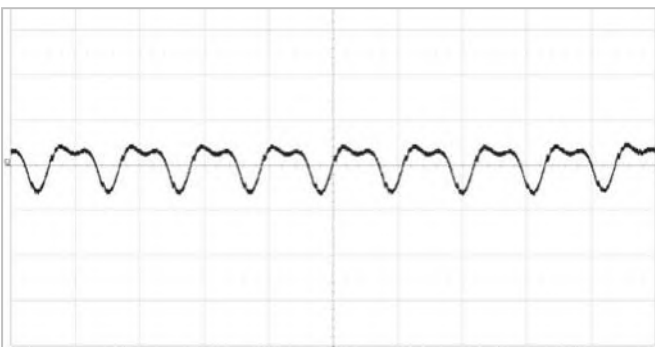
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

**Power dissipation**



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

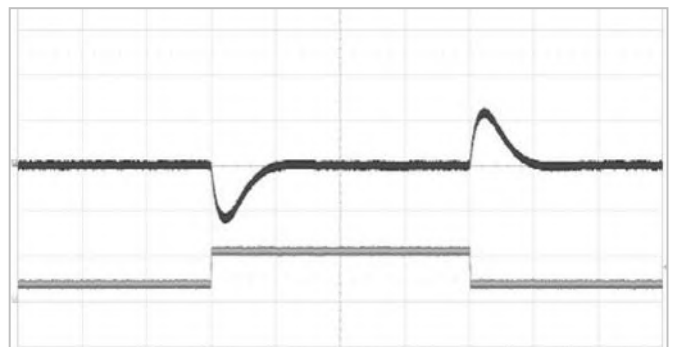
**Output ripple and noise**



Output voltage ripple at  $V_I=12\text{V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 10 mV/div, 2  $\mu\text{s}/\text{div}$ , 20 MHz bandwidth

**Transient response**



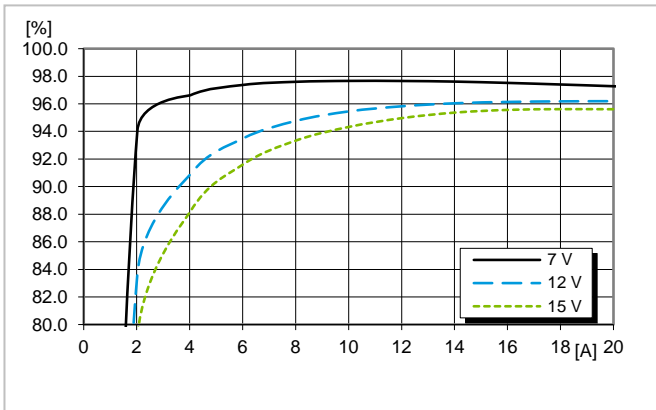
Output voltage response to output current change (7.5-22.5-7.5 A) at  $V_I=12\text{V}$ ,  $C_o=8 \times 100 \mu\text{F}$  ceramic +  $4 \times 470 \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{A}/\mu\text{s}$ .

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}/\text{div}$

### Electrical graphs for BMR4731001 (Horizontal SMD)

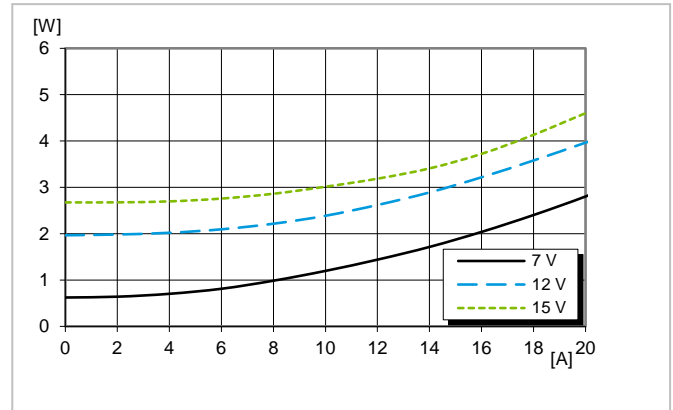
$V_{out} = 5.0\text{ V}$

#### Efficiency



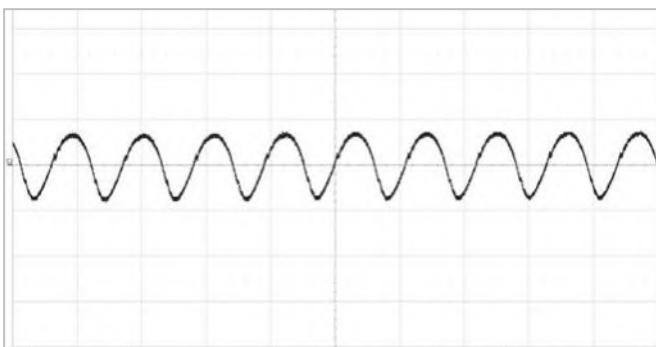
Efficiency vs. output power and input voltage at  $T_{P1} = +25^{\circ}\text{C}$

#### Power dissipation



Dissipated power vs. load power at  $T_{P1} = +25^{\circ}\text{C}$

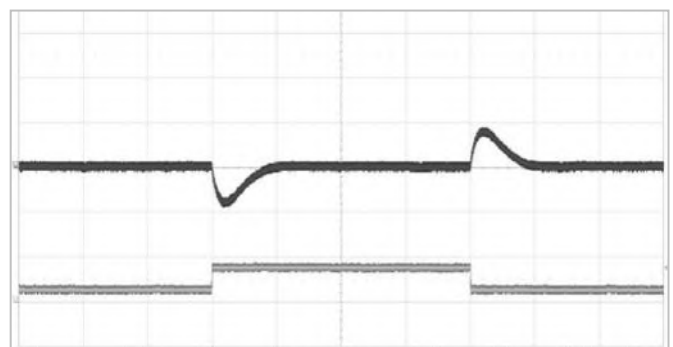
#### Output ripple and noise



Output voltage ripple at  $V_I=12\text{ V}$ ,  $I_o=\text{max } I_o$ ,  $T_{P1} = +25^{\circ}\text{C}$

Scale: 10 mV/div, 2  $\mu\text{s}$ /div, 20 MHz bandwidth

#### Transient response



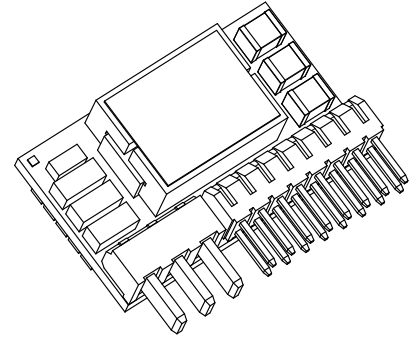
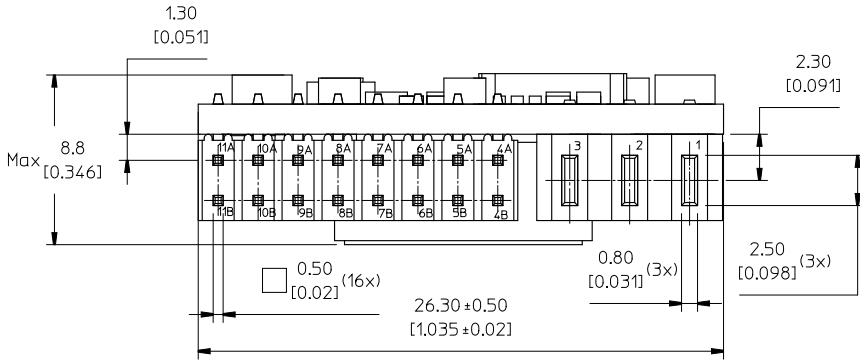
Output voltage response to output current change (5-15-5 A) at  $V_I=12\text{ V}$ ,  $C_o=8 \times 100\ \mu\text{F}$  ceramic +  $4 \times 470\ \mu\text{F}$  POSCAP (ESR 10 m $\Omega$ ),  $T_{P1} = +25^{\circ}\text{C}$ ,  $di/dt=2\text{ A}/\mu\text{s}$ .

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500  $\mu\text{s}$ /div

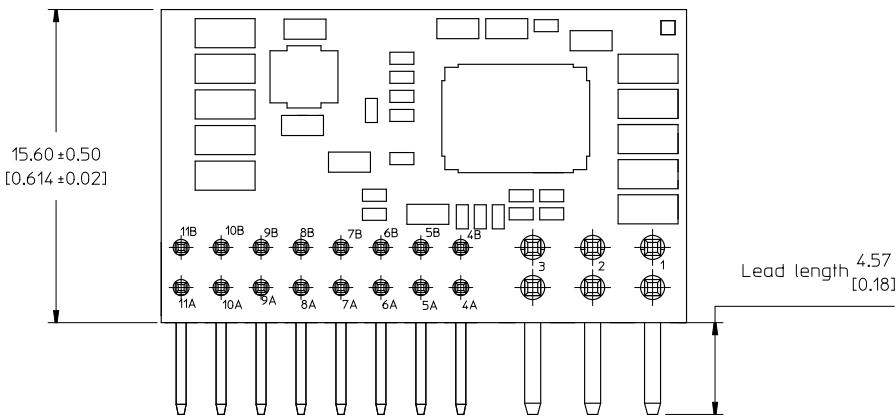
**Part 2: Mechanical information**  
**BMR473: hole mounted, Vertical SIP version**

BOTTOM VIEW

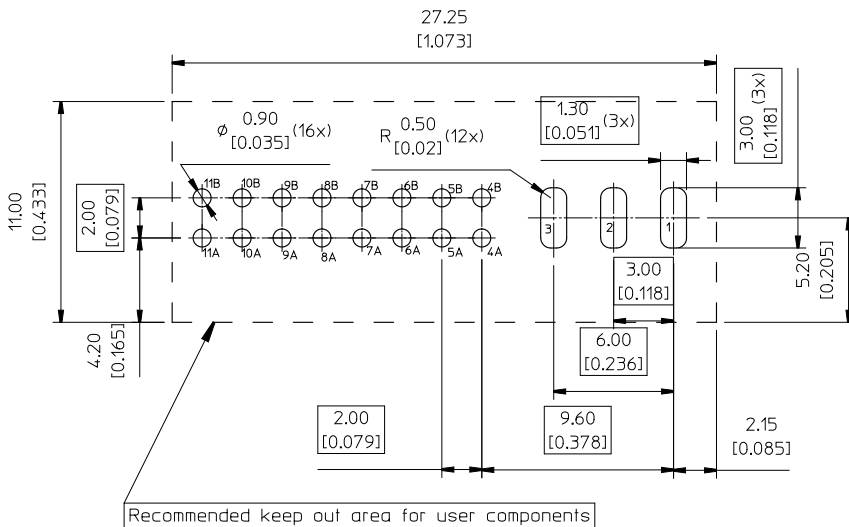
Pin positions according to recommended footprint



FRONT VIEW



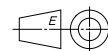
RECOMMENDED FOOTPRINT - TOP VIEW



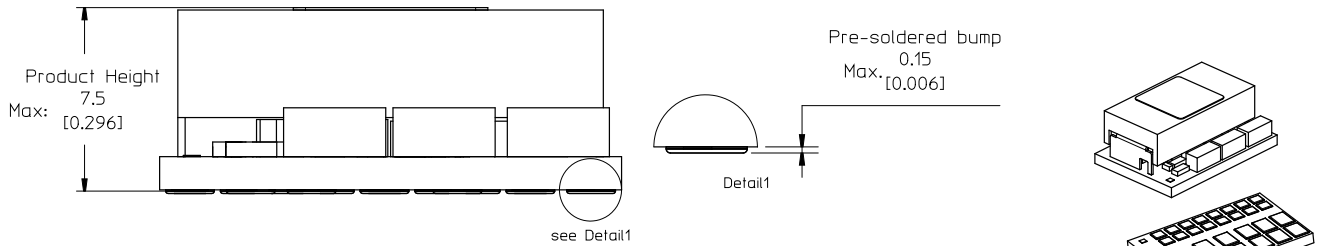
PIN SPECIFICATIONS

Pin 1-3 Material: Copper alloy (C11000)  
Plating: Min Au 0.1 µm over 1-3 µm Ni.  
Pin 4A-11B Material: Copper alloy  
Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 8.5 g  
All dimensions in mm [inch]  
Tolerances unless specified:  
x.x ± 0.50 [0.02]  
x.xx ± 0.25 [0.01]  
(not applied on footprint or typical values)

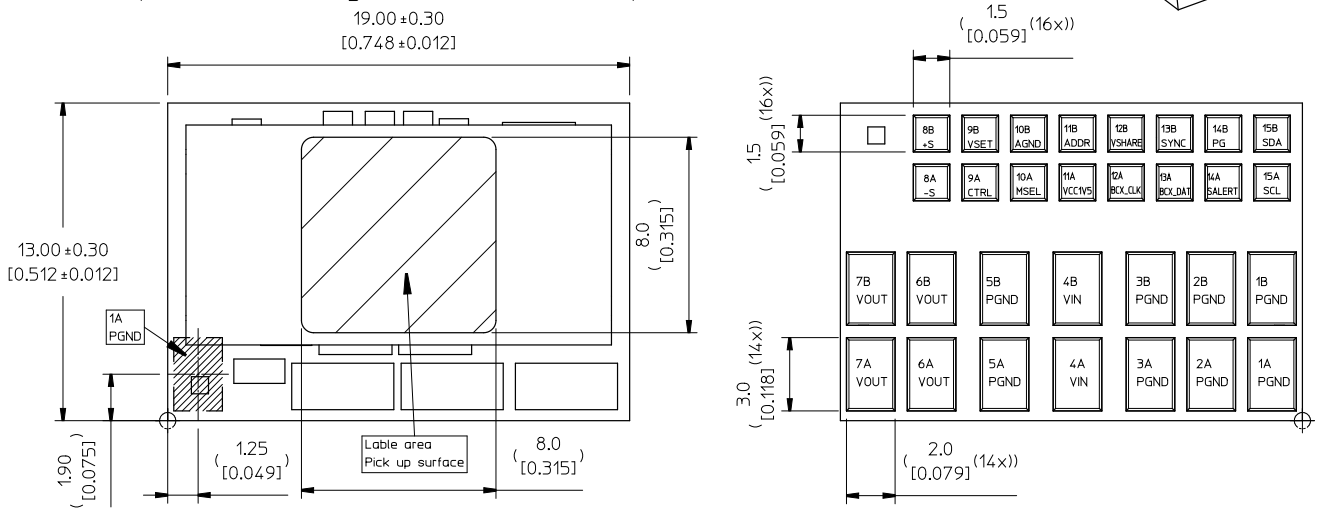


**Part 2: Mechanical information**  
**BMR473: Horizontal Surface Mount version**

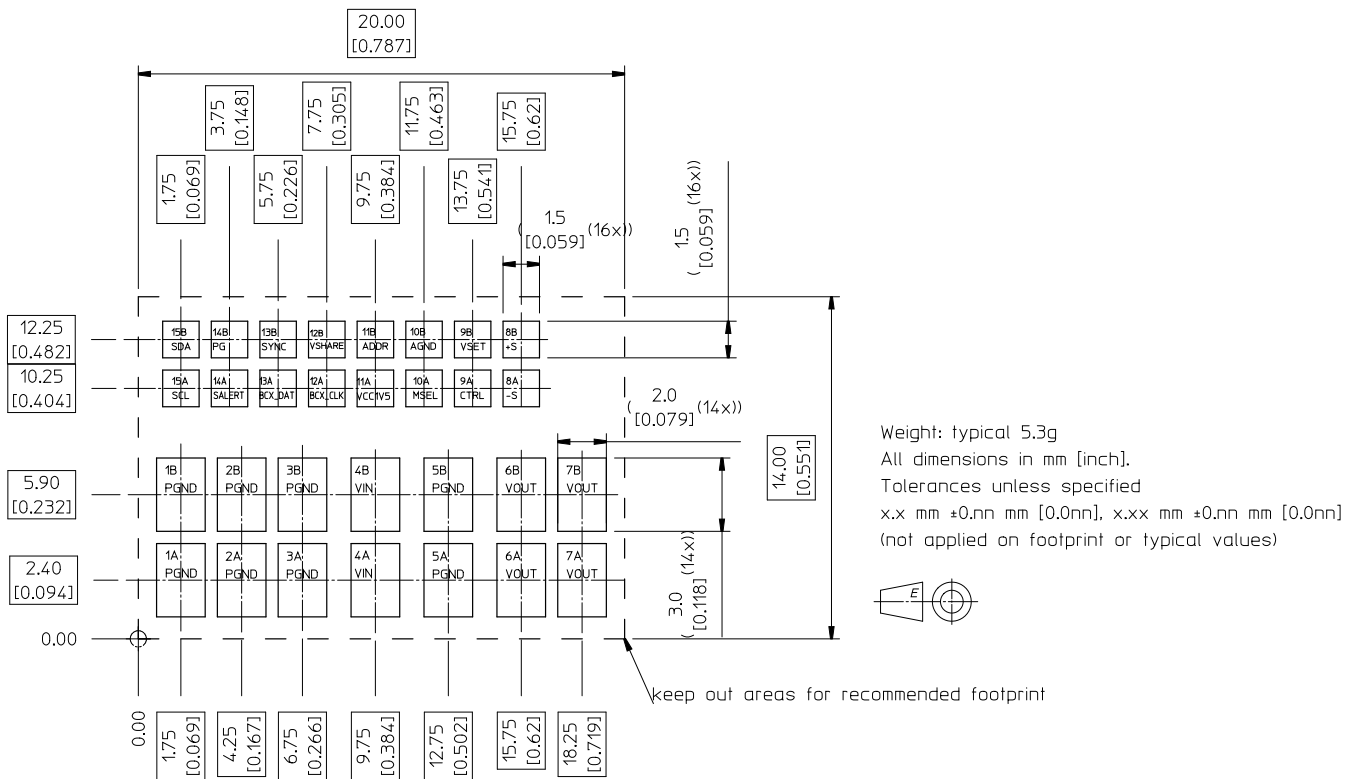


TOP VIEW

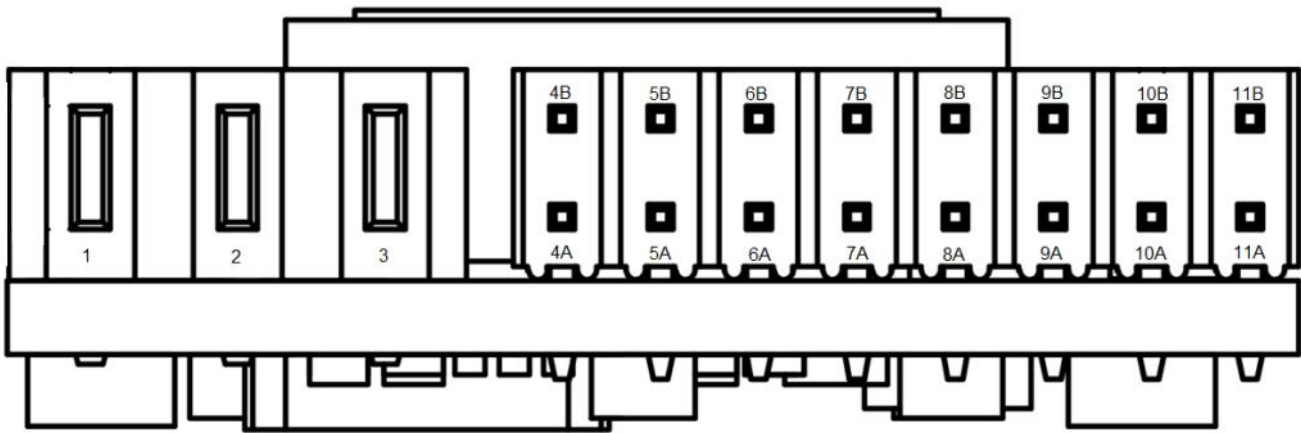
Pin position according to recommended footprint



RECOMMENDED FOOTPRINT - TOP VIEW

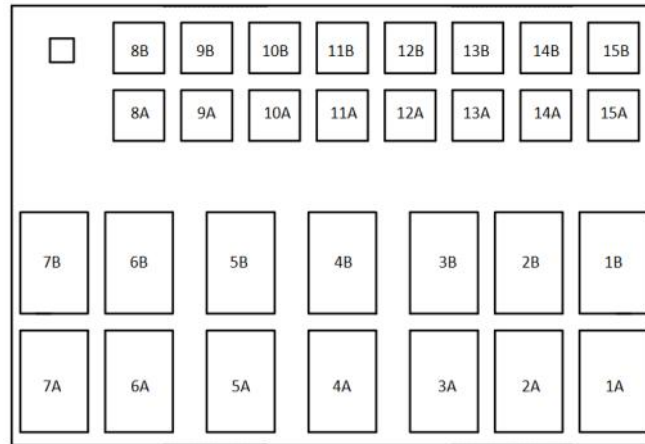


## Connections for BMR4732001 (Vertical SIP)



Pin layout, bottom view, SIP

Pin	Designation	Type	Function
1	VIN	Power	Input voltage
2	GND	Power	Power ground
3	VOUT	Power	Output voltage
4A	SALERT	O, Open drain	PMBus Alert
4B	SCL	I/O	PMBus Clock
5A	SDA	I/O	PMBus Data
5B	PG	O, Open drain	PowerGood output
6A	BCX_DAT	I/O	Back-channel communications data
6B	BCX_CLK	I/O	Back-channel communications clock
7A	SYNC	I/O	Switching frequency synchronization
7B	VCC1V5	Power	Reference voltage for pin strapping
8A	AGND	Power	Ground reference for pin strapping
8B	VSHARE	I/O	Voltage sharing for paralleling
9A	VSET	I	Output voltage pin strap
9B	ADDR	I	PMBus address pin strap
10A	+S	I	Positive sense
10B	MSEL	I	Pin strap for soft-start time, over current fault limit and paralleling.
11A	-S	I	Negative sense
11B	CTRL	I	Remote Control

**Connections for BMR4731001 (Horizontal SMD)**

Pin layout, bottom view, horizontal mount SMD

Pin	Designation	Type	Function
1A,1B,2A,2B,3A,3B	GND	Power	Power ground
4A,4B	VIN	Power	Input voltage
5A,5B	GND	Power	Power ground
6A,6B,7A,7B	VOUT	Power	Output voltage
8A	-S	I	Negative sense
8B	+S	I	Positive sense
9A	CTRL	I	Remote Control
9B	VSET	I	Output voltage pin strap
10A	MSEL	I	Pin strap for soft-start time, over current fault limit and paralleling.
10B	AGND	Power	Ground reference for pin strapping
11A	VCC1V5	Power	Reference voltage for pin strapping
11B	ADDR	I	PMBus address pin strap
12A	BCX_CLK	I/O	Back-channel communications clock
12B	VSHARE	I/O	Voltage sharing for paralleling
13A	BCX_DAT	I/O	Back-channel communications data
13B	SYNC	I/O	Switching frequency synchronization
14A	SALERT	O, Open drain	PMBus Alert
14B	PG	O, Open drain	PowerGood output
15A	SCL	I/O	PMBus Clock
15B	SDA	I/O	PMBus Data

## Part 3: Thermal considerations

### Thermal considerations

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

#### General

Cooling is mainly achieved by conduction from the pins to the host board and convection which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The products comes in a vertical SIP as well as horizontally mounted SMD version. For products mounted on a PWB without a heatsink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product. The wind speed and temperature are measured in a point upstream of the device. Distances between the tested device and the top space board and the side airflow guides are  $6.35 \text{ mm} \pm 1 \text{ mm}$ .

The product is tested on a  $254 \times 254 \text{ mm}$ ,  $35 \mu\text{m}$  (1 oz), 8 layer test board mounted vertically in a wind tunnel with a cross section of  $608 \times 203 \text{ mm}$ .

The [output current derating graphs](#) found later in this section for each model provide the available output current vs. ambient air temperature and air velocity at  $V_{in} = 12 \text{ V}$ .

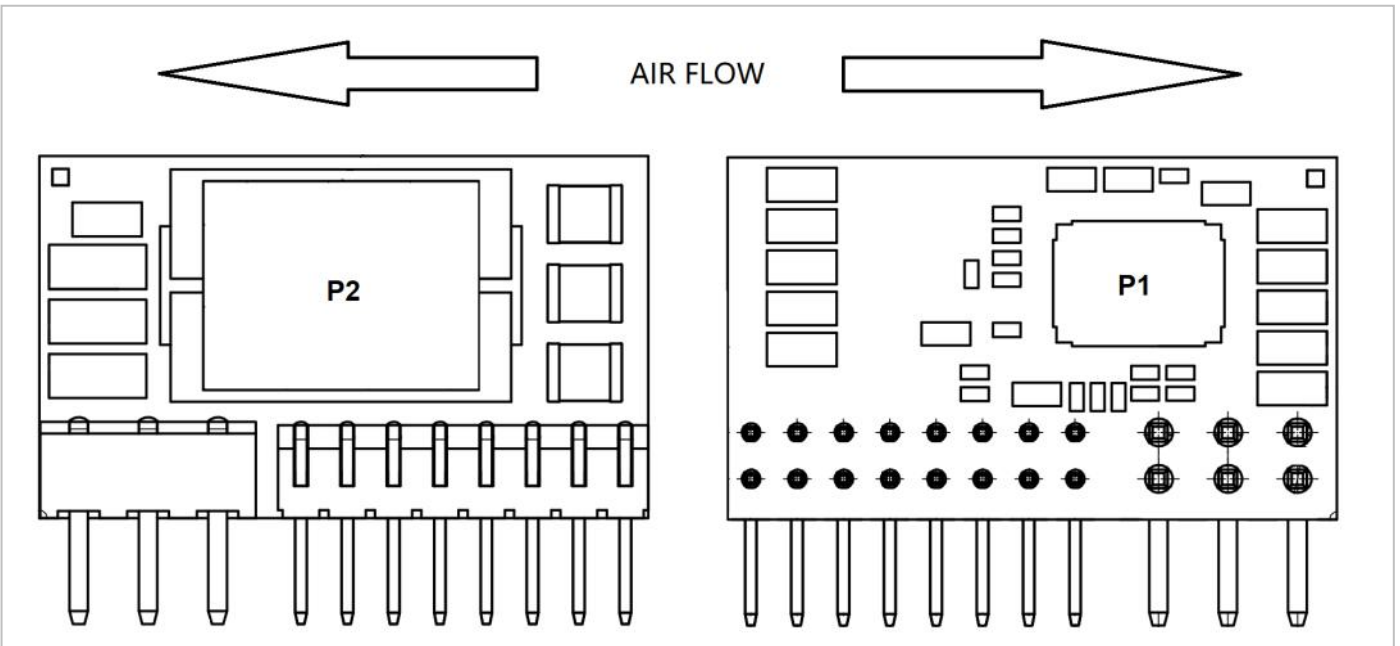
#### Definition of product operating temperature

Proper thermal conditions can be verified by measuring the temperature at position P1 as shown below. The temperature at this position ( $T_{P1}$ ) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum  $T_{P1}$ , measured at the reference point P1 are not allowed and may cause permanent damage.

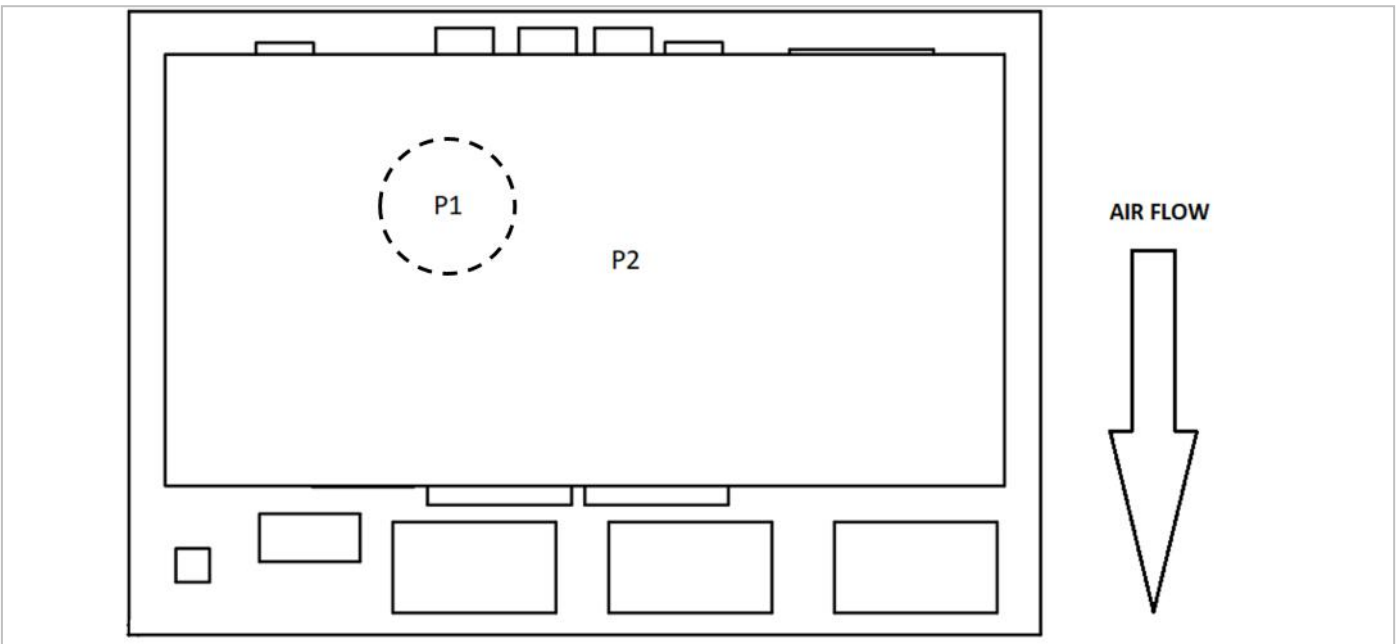
SIP Mounting		
Position	Description	Max. Temp.
P1	Controller	$T_{P1} = 125 \text{ }^\circ\text{C}$
P2	Inductor	$T_{P2} = 125 \text{ }^\circ\text{C}$

Horizontal Mounting		
Position	Description	Max. Temp.
P1	Controller	$T_{P1} = 125 \text{ }^\circ\text{C}$
P2	Inductor	$T_{P2} = 125 \text{ }^\circ\text{C}$

Temperature position and air flow direction



Temperature position and air flow direction, Vertical SIP

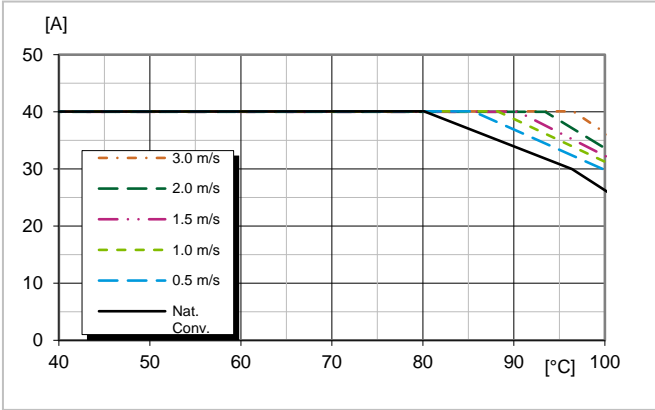


Temperature position and air flow direction, Horizontal mount SMD

Thermal graphs for BMR4732001 (Vertical SIP)

$V_{out} = 0.6\text{ V}$

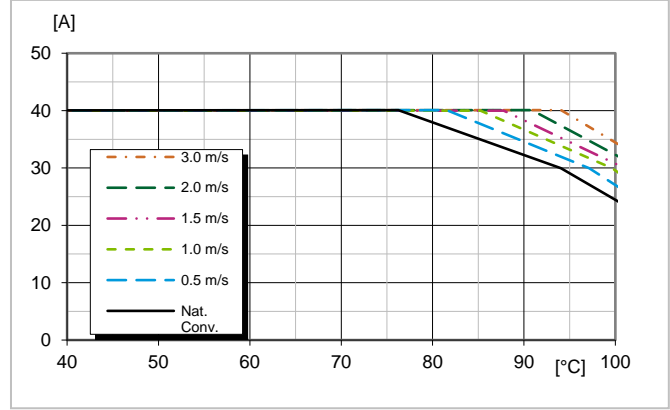
Output current derating - open frame



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{ V}$ ,  $V_o = 0.6\text{ V}$ .

$V_{out} = 1.0\text{ V}$

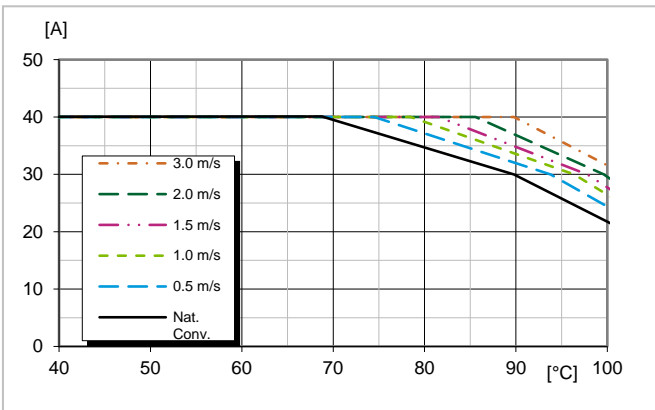
Output current derating - open frame



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{ V}$ ,  $V_o = 1.0\text{ V}$ .

$V_{out} = 1.8\text{ V}$

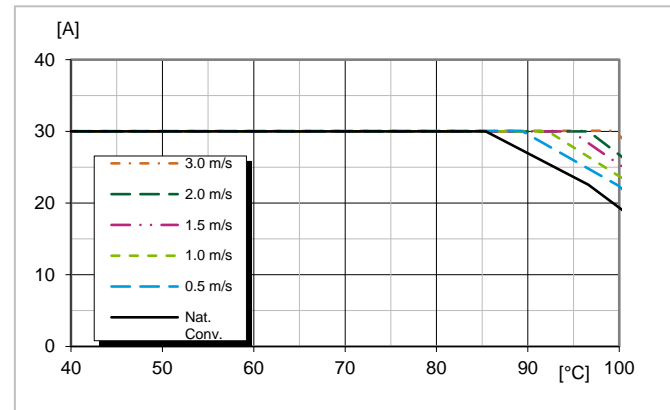
Output current derating - open frame



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{ V}$ ,  $V_o = 1.8\text{ V}$ .

$V_{out} = 2.5\text{ V}$

Output current derating - open frame

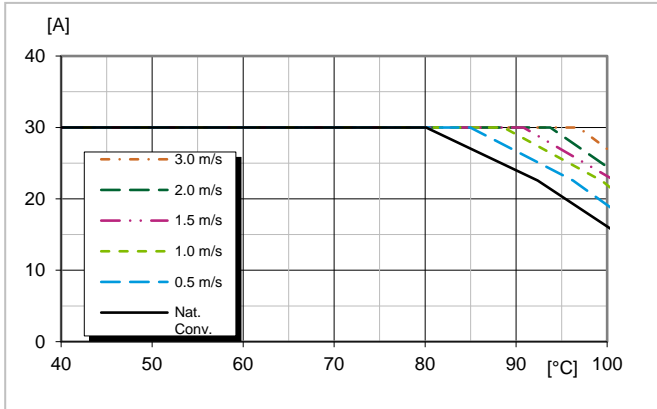


Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{ V}$ ,  $V_o = 2.5\text{ V}$ .

Thermal graphs for BMR4732001 (Vertical SIP)

$V_{out} = 3.3\text{ V}$

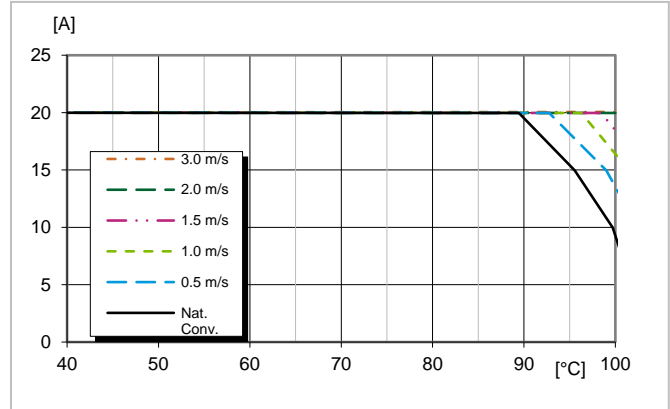
Output current derating - open frame



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 3.3\text{V}$ .

$V_{out} = 5.0\text{ V}$

Output current derating - open frame

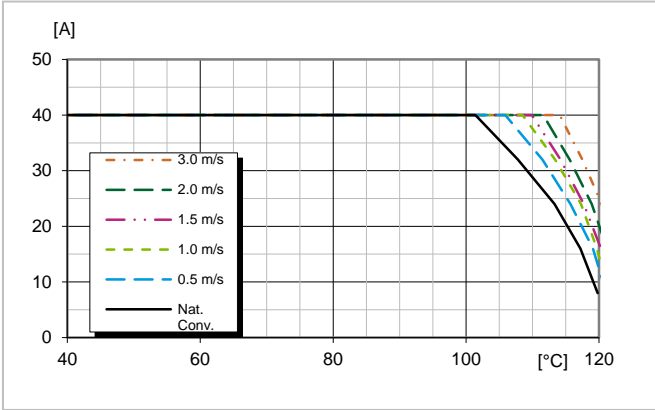


Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 5.0\text{V}$ .

**Thermal graphs for BMR4731001 (Horizontal SMD)**

**$V_{out} = 0.6\text{ V}$**

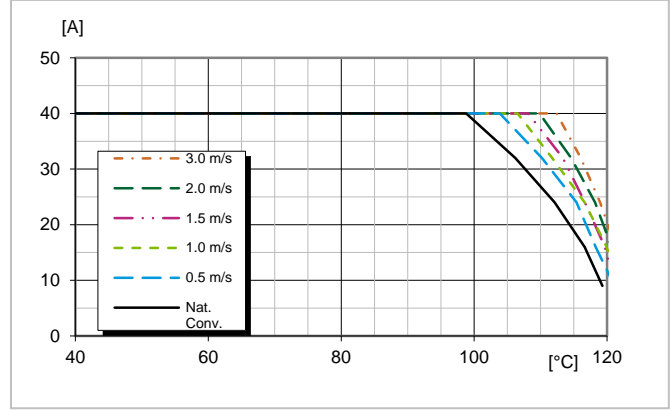
**Output current derating - open frame**



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 0.6\text{V}$ .

**$V_{out} = 1.0\text{ V}$**

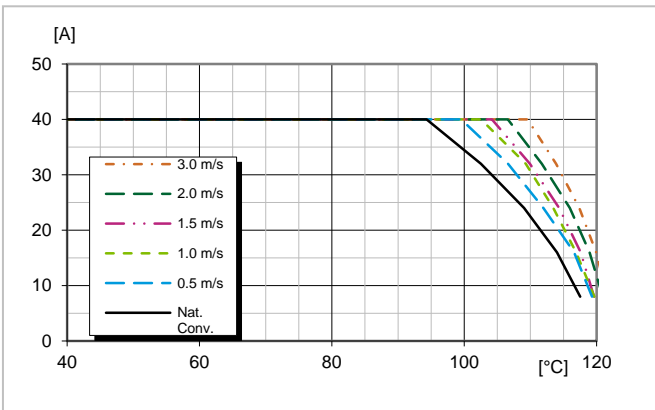
**Output current derating - open frame**



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 1.0\text{V}$ .

**$V_{out} = 1.8\text{ V}$**

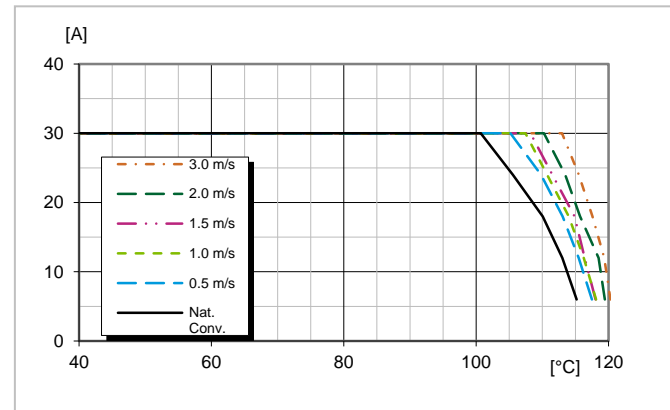
**Output current derating - open frame**



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 1.8\text{V}$ .

**$V_{out} = 2.5\text{ V}$**

**Output current derating - open frame**

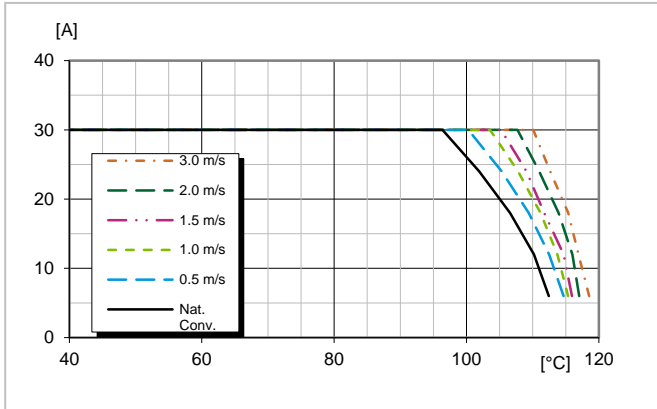


Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 2.5\text{V}$ .

**Thermal graphs for BMR4731001 (Horizontal SMD)**

**$V_{out} = 3.3\text{ V}$**

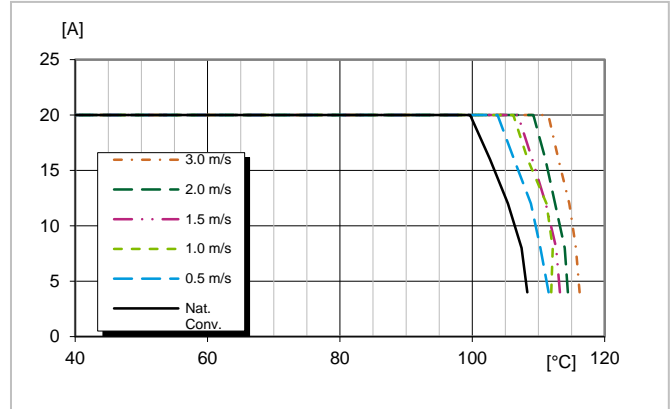
**Output current derating - open frame**



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 3.3\text{V}$ .

**$V_{out} = 5.0\text{ V}$**

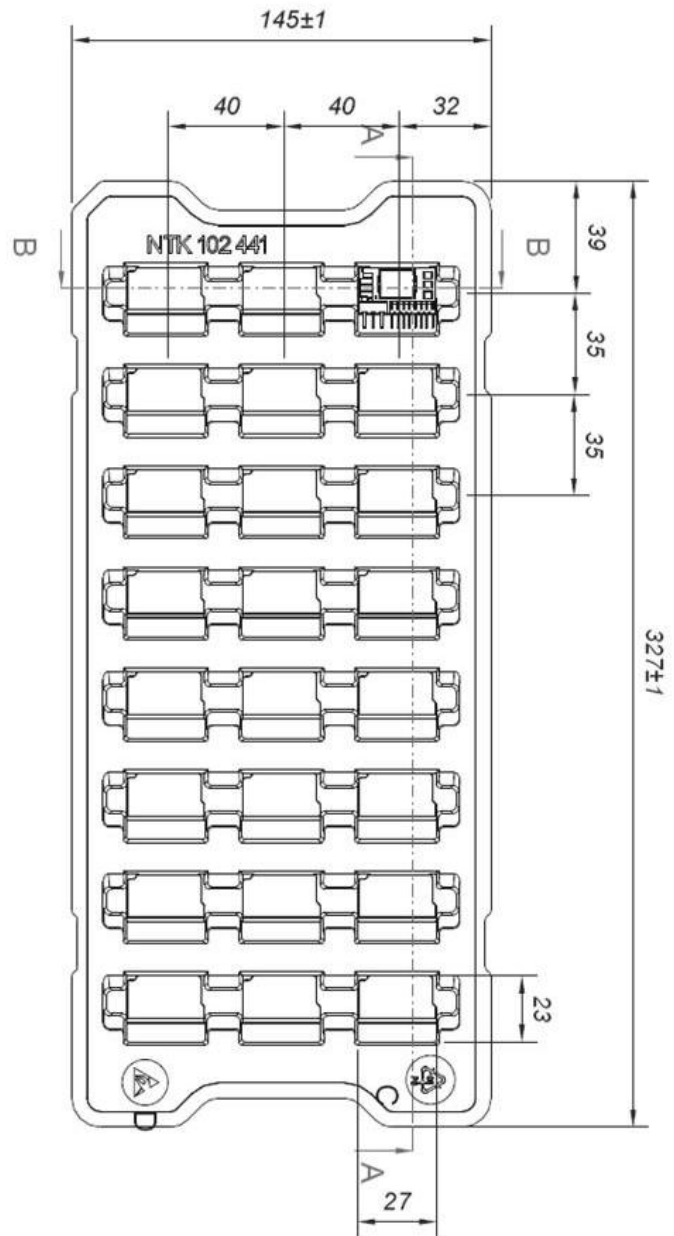
**Output current derating - open frame**



Available output current vs. ambient air temperature and airflow,  $V_i = 12\text{V}$ ,  $V_o = 5.0\text{V}$ .

**Part 4: Packaging**  
**Packaging information— Vertical SIP**

B option:	
<b>Material</b>	Antistatic Polystyrene (black)
<b>Surface resistance</b>	$10^5 < \text{ohm/square} < 10^{11}$
<b>Bakability</b>	Trays are not bakeable
<b>Tray thickness</b>	20 mm (0.787 in) for SIP version
<b>Box capacity</b>	240 products (10 full trays/box)
<b>Tray weight</b>	47g empty tray, 255g full tray (SIP version)



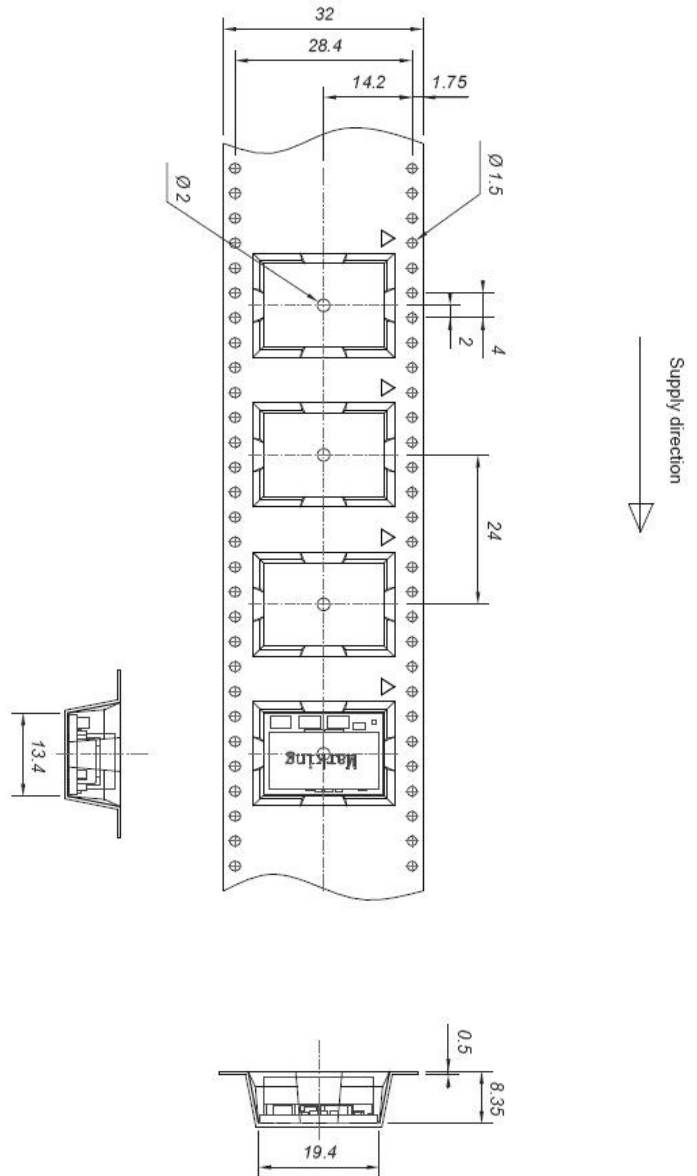
All dimensions in mm [inch]

Tolerances: X.x ±0.26 [0.01], X.xx ±0.13 [0.005]

**Note:** The tray is not designed for machine pick up

**Part 4: Packaging**  
Packaging information— Horizontal SMD

C option:	
<b>Material</b>	Antistatic Polystyrene (black)
<b>Surface resistance</b>	$10^5 < \text{ohm/square} < 10^{11}$
<b>Bakability</b>	Trays are not bakeable
<b>Tape width, W</b>	32 mm [1.26 inch]
<b>Pocket pitch, P<sub>1</sub></b>	24 mm [0.94 inch]
<b>Pocket depth, K<sub>0</sub></b>	8.35 mm [0.33 inch]
<b>Reel diameter</b>	381 mm [15 inch]
<b>Reel capacity</b>	200 products /reel
<b>Reel weight</b>	1.5 kg/full reel



## Part 5: Revision history

### Revision table

Revision number	revision change	date	revisor
Rev. A	First release edition.	2022-06-30	JIDMWANG
Rev. B	Add variant of BMR4731001	2023-01-05	JIDMWANG
Rev. C	Minor changes	2024-01-26	KARWAER
Rev. D	Update pin description in	2025-02-04	JIDJLAA

© Flex Power Modules 2025

The information and specifications in this technical specification is believed to be correct at the time of publication. However, no liability is accepted for inaccuracies, printing errors or for any consequences thereof. Flex Power Modules reserves the right to change the contents of this technical specification at any time without prior notice.

## TECHNICAL REFERENCE DOCUMENT: GENERAL INFORMATION

### Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the *RoHS directive 2011/65/EU* and *2015/863* have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, DIBP and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power Modules products are found in the [Statement of Compliance document](#).

Flex Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals ([REACH](#)) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

### Quality statement

The products are designed and manufactured in an industrial environment where quality systems and methods like [ISO 9001](#), [ISO 14001](#), [ISO 45001](#), *Six Sigma*, and *SPC* are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged workforce, contribute to the high quality of the products.

### Warranty

Warranty period and conditions are defined in *Flex Power Modules' General Terms and Conditions of Sales*.

### Limitation of Liability

Flex Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

## Product qualification specifications

Characteristics			
External visual inspection	IPC-A-610		
Temperature shock test (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 125°C 700 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T <sub>A</sub> Duration	-45°C 72 hr
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85% RH 1000 hr
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 hr
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Fluxcleaner Isopropyl alcohol	55°C 23° C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture classification and reflow sensitivity <sup>1</sup>	J-STD-020E	Level 3 (Pb Free)	245°C
Operational Life test Rapid Temp.	MIL-STD-202G, method 108A	Duration	1000 hr
Resistance to soldering heat <sup>2</sup>	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability (through hole)	IEC 60068-2-20 test T <sub>a</sub>	Preconditioning Temperature, Pb-free	Steam ageing 245°C
Solderability (surface mount)	IEC 60068-2-58 test T <sub>d</sub>	Preconditioning Temperature, Pb-free	Steam ageing 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g <sup>2</sup> /Hz 10 min in each direction

Note 1: only for products intended for reflow soldering (surface mount products & pin-in paste products)

Note 2: only for products intended for wave soldering (plated through hole products)

## TECHNICAL REFERENCE DOCUMENT: SOLDERING

### Reflow soldering profile for surface mount and pin-in-paste assembly

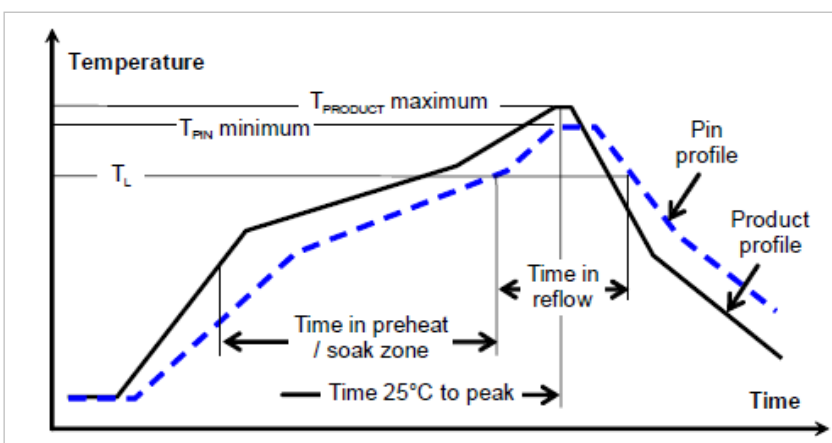
Products intended for surface mount or pin-in-paste assembly are qualified for use in a Pb-free forced convection or vapor phase reflow soldering process.

For Pb-free solder processes, a pin temperature ( $T_{pin}$ ) in excess of the solder melting temperature ( $T_L$ , 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

The preferred method for soldering through-hole mount products is wave solder. If pin-in-paste reflow soldering is used, exposure above the maximum peak temperature of 245 °C or exceeding the maximum reflow time above  $T_L$  must be avoided to ensure long term reliability. The power module temperatures must be measured via thermocouple at a minimum of 2 locations.

$T_L$  is the typical solder melting (liquidous) temperature  
 $T_{product}$  is measured on the power module's hotspot  
 $T_{pin}$  is measured on the power module output power pins solder joints at the customer board

General reflow process specification		Pb-free, SAC305
Average ramp-up rate ( $T_{product}$ )		3 °C/s max
Typical solder melting temp.	$T_L$	217 °C
Min/Max. reflow time above $T_L$	$T_{pin}$	60 –150 s
Min. pin temp.	$T_{pin}$	235 °C
Peak product temp.	$T_{product}$	245 °C
Average ramp-down ( $T_{product}$ )		6°C/s max
Max. time 25° C to peak		8 minutes



Typical soldering profile

## Wave and manual soldering information - through-hole mounting

The through-hole mounted product is intended for solder attachment by wave or manual soldering. The pin temperature is specified for 270°C peak for maximum 10 seconds.

A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, be careful to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

## Moisture reflow classification

For Pb-free reflow solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

For wave solder processes, the moisture sensitivity level does not apply.

## Dry pack information

Using products in high temperature reflow soldering processes requires dry pack storage and handling. Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices). In case the products have been stored in an uncontrolled environment and no longer can be considered dry, floor life according to MSL 3, the modules must be baked according to J-STD-033.

## Post solder cleaning

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long term reliability and isolation voltage.

## TECHNICAL REFERENCE DOCUMENT: SAFETY

### Safety specifications

Flex Power Modules' DC/DC converters and DC/DC regulators are designed in accordance with the safety standards *IEC 62368-1*, *EN 62368-1* and *UL 62368-1 Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power Interface Modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "conditions of acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (please refer to *Technical Specification under Mechanical Information* for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use shall comply with the requirements in *IEC/EN/UL 62368-1*. Product related standards, e.g. *IEEE 802.3af Power over Ethernet*, and *ETS-300132-2 Power interface at the input to telecom equipment, operated by direct current (dc)* are based on *IEC/EN/UL 62368-1* with regards to safety.

All Flex Power Modules' DC/DC converters, Power Interface Modules and DC/DC regulators are recognized and certified in accordance with *IEC/EN/UL 62368-1*. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to *IEC 62368-1 10 Fire hazard testing, test flames – 50 W horizontal and vertical flame test methods*.

### Non-isolated DC/DC regulators

The DC/DC regulator output is ES1 energy source if the input source meets the requirements for ES1 according to *IEC/EN/UL 62368-1*.

## Technical Reference PMBus BMR473

This appendix contains a detailed reference of the PMBus commands supported by the product.

### Data Formats

The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

### Standard Commands

The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

### Forum Websites

The System Management Interface Forum (SMIF)

<http://www.powersig.org/>

The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum  
(PMBUS-IF)

<http://pmbus.org/>

The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

### PMBus – Power System Management Bus Protocol Documents

These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport And Electrical Interface

Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language

Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

### SMBus – System Management Bus Documents

System Management Bus Specification, Version 2.0, August 3, 2000

This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:

<http://www.smbus.org/specs/>

## PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Flex Power Designer tool.

Code	Name	Data Format	Factory Default Value Standard Configuration BMR4731X01/001 R1		Min Set Value	Max Set Value	Unit
0x01	OPERATION	R/W Byte	0x04				
0x02	ON_OFF_CONFIG	R/W Byte	0x17				
0x03	CLEAR_FAULTS	Send Byte					
0x04	PHASE	R/W Byte					
0x10	WRITE_PROTECT	R/W Byte	0x00				
0x15	STORE_USER_ALL (Phase 0xFF)	Send Byte					
0x16	RESTORE_USER_ALL (Phase 0xFF)	Send Byte					
0x19	CAPABILITY	Read Byte					
0x1B	SMBALERT_MASK_VOUT (STATUS_VOUT)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_VOUT (Phase 0xFF)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_IOUT (STATUS_IOUT)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_IOUT (Phase 0xFF)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_INPUT (STATUS_INPUT)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_INPUT (Phase 0xFF)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_TEMPERATU RE (STATUS_TEMPERATURE)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_TEMPERATU RE (Phase 0xFF)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_CML (STATUS_CML)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_CML (Phase 0xFF)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_MFR_SPECIFI C (STATUS_MFR_SPECIFIC)	SMBAlert Mask	0x00				
0x1B	SMBALERT_MASK_MFR_SPECIFI C (Phase 0xFF)	SMBAlert Mask	0x00				
0x20	VOUT_MODE	Read Byte	0x97				
0x21	VOUT_COMMAND	R/W Word	1 x Vout by pin-strap				
0x22	VOUT_TRIM	R/W Word	Unit Specific				
0x24	VOUT_MAX	R/W Word	Configured by pin-strap		0.6	6.0	V
0x25	VOUT_MARGIN_HIGH	R/W Word	0x021A	1.05			* Vout
0x26	VOUT_MARGIN_LOW	R/W Word	0x01E6	0.95			* Vout
0x27	VOUT_TRANSITION_RATE	R/W Word	0xE010	1.00	0.067	15.933	V/ms
0x29	VOUT_SCALE_LOOP	R/W Word	Configured by pin-strap				

0x2B	VOUT_MIN	R/W Word	Configured by pin-strap		0.5	5.0	V
0x33	FREQUENCY_SWITCH	R/W Word	0x01C2	450.00	450	900	kHz
0x35	VIN_ON	R/W Word	0xF016	5.50	5.5	15	V
0x36	VIN_OFF	R/W Word	0xF012	4.50	4.5	15	V
0x37	INTERLEAVE	R/W Word					
0x38	IOUT_CAL_GAIN	R/W Word	Unit Specific				
0x39	IOUT_CAL_OFFSET (Phase 0)	R/W Word	Unit Specific				
0x39	IOUT_CAL_OFFSET (Phase 1)	R/W Word	Unit Specific				
0x39	IOUT_CAL_OFFSET (Phase 2)	R/W Word	Unit Specific				
0x39	IOUT_CAL_OFFSET (Phase 3)	R/W Word	Unit Specific				
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	0x024C	1.15			* Vout
0x41	VOUT_OV_FAULT_RESPONSE	R/W Byte	0xBF				
0x42	VOUT_OV_WARN_LIMIT	R/W Word	0x0233	1.10			* Vout
0x43	VOUT_UV_WARN_LIMIT	R/W Word	0x01CC	0.90			* Vout
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	0x01B3	0.85			* Vout
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	0xBF				
0x46	IOUT_OC_FAULT_LIMIT (Phase 0)	R/W Word	0xF0D0	52.00	8	52	A
0x46	IOUT_OC_FAULT_LIMIT (Phase 1)	R/W Word	0xF0D0	52.00	8	52	A
0x46	IOUT_OC_FAULT_LIMIT (Phase 2)	R/W Word	0xF0D0	52.00	8	52	A
0x46	IOUT_OC_FAULT_LIMIT (Phase 3)	R/W Word	0xF0D0	52.00	8	52	A
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	0xBF				
0x4A	IOUT_OC_WARN_LIMIT (Phase 0)	R/W Word	0xF0A0	40.00	8	52	A
0x4A	IOUT_OC_WARN_LIMIT (Phase 1)	R/W Word	0xF0A0	40.00	8	52	A
0x4A	IOUT_OC_WARN_LIMIT (Phase 2)	R/W Word	0xF0A0	40.00	8	52	A
0x4A	IOUT_OC_WARN_LIMIT (Phase 3)	R/W Word	0xF0A0	40.00	8	52	A
0x4F	OT_FAULT_LIMIT (Phase 0)	R/W Word	0x0087	135.00	0	150	°C
0x4F	OT_FAULT_LIMIT (Phase 1)	R/W Word	0x0087	135.00	0	150	°C
0x4F	OT_FAULT_LIMIT (Phase 2)	R/W Word	0x0087	135.00	0	150	°C
0x4F	OT_FAULT_LIMIT (Phase 3)	R/W Word	0x0087	135.00	0	150	°C
0x50	OT_FAULT_RESPONSE	R/W Byte	0xBF				
0x51	OT_WARN_LIMIT (Phase 0)	R/W Word	0x007D	125.00	0	150	°C
0x51	OT_WARN_LIMIT (Phase 1)	R/W Word	0x007D	125.00	0	150	°C
0x51	OT_WARN_LIMIT (Phase 2)	R/W Word	0x007D	125.00	0	150	°C
0x51	OT_WARN_LIMIT (Phase 3)	R/W Word	0x007D	125.00	0	150	°C
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0x0010	16.00	6	16	V
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0xBF				
0x58	VIN_UV_WARN_LIMIT (Phase 0)	R/W Word	0xF016	5.50	4	11.25	V
0x58	VIN_UV_WARN_LIMIT (Phase 1)	R/W Word	0xF016	5.50	4	11.25	V
0x58	VIN_UV_WARN_LIMIT (Phase 2)	R/W Word	0xF016	5.50	4	11.25	V

0x58	VIN_UV_WARN_LIMIT (Phase 3)	R/W Word	0xF016	5.50	4	11.25	V
0x60	TON_DELAY	R/W Word	0xF814	10.00	0	127.5	ms
0x61	TON_RISE	R/W Word	0xF028	10.00	0	31.75	ms
0x62	TON_MAX_FAULT_LIMIT	R/W Word	0xF800	0.00			ms
0x63	TON_MAX_FAULT_RESPONSE	R/W Byte	0x3B				
0x64	TOFF_DELAY	R/W Word	0xF800	0.00	0	127.5	ms
0x65	TOFF_FALL	R/W Word	0xF002	0.50	0	31.75	ms
0x78	STATUS_BYTE (Phase 0)	Read Byte					
0x78	STATUS_BYTE (Phase 1)	Read Byte					
0x78	STATUS_BYTE (Phase 2)	Read Byte					
0x78	STATUS_BYTE (Phase 3)	Read Byte					
0x79	STATUS_WORD (Phase 0)	R/W Word					
0x79	STATUS_WORD (Phase 1)	R/W Word					
0x79	STATUS_WORD (Phase 2)	R/W Word					
0x79	STATUS_WORD (Phase 3)	R/W Word					
0x7A	STATUS_VOUT	R/W Byte					
0x7B	STATUS_IOUT (Phase 0)	R/W Byte					
0x7B	STATUS_IOUT (Phase 1)	R/W Byte					
0x7B	STATUS_IOUT (Phase 2)	R/W Byte					
0x7B	STATUS_IOUT (Phase 3)	R/W Byte					
0x7C	STATUS_INPUT (Phase 0)	R/W Byte					
0x7C	STATUS_INPUT (Phase 1)	R/W Byte					
0x7C	STATUS_INPUT (Phase 2)	R/W Byte					
0x7C	STATUS_INPUT (Phase 3)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 0)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 1)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 2)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 3)	R/W Byte					
0x7E	STATUS_CML (Phase 0)	R/W Byte					
0x7E	STATUS_CML (Phase 1)	R/W Byte					
0x7E	STATUS_CML (Phase 2)	R/W Byte					
0x7E	STATUS_CML (Phase 3)	R/W Byte					
0x7F	STATUS_OTHER	Read Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 0)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 1)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 2)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 3)	R/W Byte					
0x88	READ_VIN (Phase 0)	Read Word					
0x88	READ_VIN (Phase 1)	Read Word					
0x88	READ_VIN (Phase 2)	Read Word					
0x88	READ_VIN (Phase 3)	Read Word					
0x8B	READ_VOUT (Phase 0)	Read Word					
0x8B	READ_VOUT (Phase 1)	Read Word					
0x8B	READ_VOUT (Phase 2)	Read Word					
0x8B	READ_VOUT (Phase 3)	Read Word					
0x8C	READ_IOUT (Phase 0)	Read Word					

0x8C	READ_IOUT (Phase 1)	Read Word					
0x8C	READ_IOUT (Phase 2)	Read Word					
0x8C	READ_IOUT (Phase 3)	Read Word					
0x8C	READ_IOUT (Per Rail)	Read Word					
0x8D	READ_TEMPERATURE_1 (Phase 0)	Read Word					
0x8D	READ_TEMPERATURE_1 (Phase 1)	Read Word					
0x8D	READ_TEMPERATURE_1 (Phase 2)	Read Word					
0x8D	READ_TEMPERATURE_1 (Phase 3)	Read Word					
0x8D	READ_TEMPERATURE_1 (Per Rail)	Read Word					
0x98	PMBUS_REVISION	Read Byte					
0x99	MFR_ID	R/W Block3	Unit Specific				
0x9A	MFR_MODEL	R/W Block3	Unit Specific				
0x9B	MFR_REVISION	R/W Block3	Unit Specific				
0x9E	MFR_SERIAL	R/W Block3	Unit Specific				
0xAD	IC_DEVICE_ID	Read Block6					
0xAE	IC_DEVICE_REV	Read Block2					
0xB1	USER_DATA_01 (Phase 0xFF)	R/W Block5	0xC43FF82311				
0xD0	TELEMETRY_CONFIG	R/W Block6	0x030003030303				
0xDA	READ_ALL	Read Block14					
0xDB	STATUS_ALL	Read Block7					
0xDC	STATUS_PHASE (Phase 0xFF)	Read Word					
0xE3	PGOOD_CONFIG	R/W Word	0x006A				
0xE4	SYNC_CONFIG	R/W Byte	0xF0				
0xEC	STACK_CONFIG	R/W Word	0x0000				
0xED	MISC_OPTIONS	R/W Word	0x0000				
0xEE	PIN_DETECT_OVERRIDE	R/W Word	0x192D				
0xEF	SLAVE_ADDRESS	R/W Byte	0x14				
0xF0	NVM_CHECKSUM	Read Word					
0xF1	SIMULATE_FAULT	R/W Word	0x0000				

**PMBus Command Details****OPERATION (0x01)**

Description: Sets the desired PMBus enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable.	00	Immediate Off	Disable immediately without controlled ramp-down or sequencing.
			01	Soft Off	Disable by controlled ramp-down timings or sequencing.
			10	Enable	Enable device to the set voltage or margin state, using ramp up timings / sequencing.
5:4	Margin	Select between margin high/low states or nominal output.	00	Nominal	Operate at nominal output voltage.
			01	Margin Low	Operate at margin low voltage set in VOUT_MARGIN_LOW.
			10	Margin High	Operate at margin high voltage set in VOUT_MARGIN_HIGH.
3:2	Act on Fault	Set 10b to act on fault or set to 01b to ignore fault.	01	Ignore Faults	Ignore Faults when in a margined state. The overvoltage/undervoltage warnings and faults are ignored and do not trigger shutdown or STATUS updates.
			10	Act on Faults	Act on Faults when in a margined state. The device will handle appropriate overvoltage/undervoltage warnings and faults and respond as programmed by the warning limit or fault response command.

**ON\_OFF\_CONFIG (0x02)**

Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation		0	Ignore CTRL pin or PMBus	Unit starts power conversion any time the input power is present regardless of the state of the CTRL pin.
			1	CTRL pin or PMBus	Device does not power up until commanded by the CTRL pin or OPERATION command.
3	PMBus Enable Mode	Controls how the device responds to the PMBus command OPERATION.	0	Ignore PMBus command	Ignores the on/off portion of the OPERATION command.
			1	Use PMBus command	Device requires on by OPERATION command to enable the output voltage.

2	Enable Pin Mode	Controls how the device responds to the CTRL pin.	0	Ignore CTRL pin	Device ignores the CTRL pin.
			1	Use CTRL pin	Device requires the CTRL pin to be asserted to enable the output voltage.
1	Enable Pin Polarity	Polarity of the CTRL pin.	0	Active Low	CTRL pin will cause device to enable when driven low.
			1	Active High	CTRL pin will cause device to enable when driven high.
0	Disable Action	CTRL pin action when commanding the output to turn off.	0	Soft Off	Use the configured turn off delay and fall time.
			1	Immediate Off	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

**CLEAR\_FAULTS (0x03)**

Description: Clears all fault status bits

**PHASE (0x04)**

Description: Used to configure, control, and monitor individual phases. The phase configuration needs to be established before any phase-dependent command can be successfully executed.

Bit	Description	Format
7:0	Selects a specific phase on a multi-phase output rail. Listed values for phase selection: 0x00 PHASE, 0x01 PHASE, 0x02 PHASE, 0x03 and 0xFF TOTAL PHASE (all phases as a single entity).	Integer Unsigned

**WRITE\_PROTECT (0x10)**

Description: The WRITE\_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation.

Bit	Description	Value	Function	Description
7:0		0x80	Disable all writes	Disable all writes except to the WRITE_PROTECT command.
		0x40	Enable operation	Disable all writes except to the WRITE_PROTECT and OPERATION commands.
		0x20	Enable control and Vout commands	Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands.
		0x00	Enable all commands	Enable writes to all commands.

**STORE\_USER\_ALL (0x15)**

Addressing: Phase

Description: Commands the device to copy the entire contents of the operating memory to the matching locations in the non-volatile user store memory.

**RESTORE\_USER\_ALL (0x16)**

Addressing: Phase

Description: Commands the device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the operating memory.

**CAPABILITY (0x19)**

Description: This command provides a way for a host system to determine some key capabilities of a PMBus device.

Bit	Function	Description	Value	Function	Description
7	Packet Error Checking	Packet error checking.	0	Not Supported	Packet Error Checking not supported.
			1	Supported	Packet Error Checking is supported.
6:5	Maximum Bus Speed	Maximum bus speed.	00	100kHz	Maximum supported bus speed is 100 kHz.
			01	400kHz	Maximum supported bus speed is 400 kHz.
			10	1MHz	Maximum supported bus speed is 1 MHz.
4	Smbalert	SMBALERT	0	No Smbalert	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol.
			1	Have Smbalert	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol.
3	Numeric Format	Numeric format.	0	LINEAR or DIRECT Format	Numeric data is in LINEAR or DIRECT format.
			1	IEEE Half Precision Floating Point Format	Numeric data is in IEEE half precision floating point format.
2	AVSBus Support	AVSBus support.	0	AVSBus Not Supported	AVSBus not supported.
			1	AVSBus Supported	AVSBus supported.

**SMBALERT\_MASK\_VOUT (0x1B)**

Status Registers: STATUS\_VOUT (0x7A)

Description: SMBALERT\_MASK bits for the STATUS\_VOUT command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Vout OV Fault		0	Pull SALERT	
			1	Ignore	
6	Vout OV Warn		0	Pull SALERT	
			1	Ignore	
5			0	Pull SALERT	

	Vout UV Warn		1	Ignore	
4	Vout UV Fault		0	Pull SALERT	
			1	Ignore	
3	Vout Min/Max Fault		0	Pull SALERT	
			1	Ignore	
2	Ton Max Fault		0	Pull SALERT	
			1	Ignore	

**SMBALERT\_MASK\_IOUT (0x1B)**

Status Registers: STATUS\_IOUT (0x7B)

Description: SMBALERT\_MASK bits for the STATUS\_IOUT command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Iout OC Fault		0	Pull SALERT	
			1	Ignore	
5	Iout OC Warn		0	Pull SALERT	
			1	Ignore	

**SMBALERT\_MASK\_INPUT (0x1B)**

Status Registers: STATUS\_INPUT (0x7C)

Description: SMBALERT\_MASK bits for the STATUS\_INPUT command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Vin Overvoltage Fault		0	Pull SALERT	
			1	Ignore	
5	Vin UV Warn		0	Pull SALERT	
			1	Ignore	
3	Low Vin Fault		0	Pull SALERT	
			1	Ignore	

**SMBALERT\_MASK\_TEMPERATURE (0x1B)**

Status Registers: STATUS\_TEMPERATURE (0x7D)

Description: SMBALERT\_MASK bits for the STATUS\_TEMPERATURE command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Overtemperature Fault		0	Pull SALERT	
			1	Ignore	
6	Overtemperature Warn		0	Pull SALERT	
			1	Ignore	

**SMBALERT\_MASK\_CML (0x1B)**

Status Registers: STATUS\_CML (0x7E)

Description: SMBALERT\_MASK bits for the STATUS\_CML command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7			0	Pull SALERT	

	Invalid Or Unsupported Command Received		1	Ignore	
6	Invalid Or Unsupported Data Received		0	Pull SALERT	
			1	Ignore	
5	Packet Error Check Failed		0	Pull SALERT	
			1	Ignore	
4	Memory Error		0	Pull SALERT	
			1	Ignore	
1	Other Communication Fault		0	Pull SALERT	
			1	Ignore	

**SMBALERT\_MASK\_MFR\_SPECIFIC (0x1B)**

Status Registers: STATUS\_MFR\_SPECIFIC (0x80)

Description: SMBALERT\_MASK bits for the STATUS\_MFR\_SPECIFIC command. The SMBALERT\_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Power-On Reset Fault		0	Pull SALERT	
			1	Ignore	
6	Power-On Self-Check		0	Pull SALERT	
			1	Ignore	
3	Reset		0	Pull SALERT	
			1	Ignore	
2	BCX fault		0	Pull SALERT	
			1	Ignore	
1	Sync fault		0	Pull SALERT	
			1	Ignore	

**VOUT\_MODE (0x20)**

Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Format
4:0	Parameter	Five bit two's complement EXPONENT for the MANTISSA delivered as the data bytes for VOUT_COMMAND in VOUT_LINEAR Mode.	Integer Signed

Bit	Function	Description	Value	Function	Description
7	Rel	Selection of Absolute or Relative data format.	1	Relative	Relative Data Format.
6:5	Mode	Selection of mode for representation of output voltage parameters.	00	Linear	Linear Mode Format.

**VOUT\_COMMAND (0x21)**

Description: Sets the nominal value of the output voltage from 0.6V to 5V.

Bit	Description	Format	Unit
15:0	Sets the nominal value of the output voltage.	Vout Mode Unsigned (Exp = -9)	V

**VOUT\_TRIM (0x22)**

Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT trim value. The range is limited to +/-31 mV.	Vout Mode Signed (Exp = -9)	V

**VOUT\_MAX (0x24)**

Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value higher than this level, the output voltage will be clamped to this level.	Vout Mode Unsigned (Exp = -9)	V

**VOUT\_MARGIN\_HIGH (0x25)**

Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin high.	Vout Mode Unsigned (Exp = -9)	* Vout

**VOUT\_MARGIN\_LOW (0x26)**

Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin low.	Vout Mode Unsigned (Exp = -9)	* Vout

**VOUT\_TRANSITION\_RATE (0x27)**

Description: Sets the transition rate when changing output voltage.

Bit	Description	Format	Unit
15:0	Configures the transition time for margining and on-the-fly VOUT_COMMAND changes.	Linear	V/ms

**VOUT\_SCALE\_LOOP (0x29)**

Description: Allows PMBus devices to map between the commanded voltage, and the voltage at the control circuit.

Bit	Description	Format
15:0	Choose scaling factor. Recommended value depending on Vout: 0.5 for Vout in range 0.5 to 1.5 V 0.25 for Vout in range 1 to 3 V 0.125 for Vout in range 2 to 6 V	Linear

**VOUT\_MIN (0x2B)**

Description: Configures the minimum allowed output voltage.

Bit	Description	Format	Unit
-----	-------------	--------	------

15:0	If the device is commanded to a Vout value lower than this level, the output voltage will be clamped to this level.	Vout Mode Unsigned (Exp = -9)	V
------	---	-------------------------------	---

**FREQUENCY\_SWITCH (0x33)**

Description: Controls the switching frequency.

Bit	Description	Format	Unit
15:0	Sets the switching frequency in kHz. The specified range is 450 - 900 kHz. The effective switching frequency is limited to a limited set of values: 450 kHz, 550 kHz, 650 kHz, 750 kHz, 900 kHz	Linear	kHz

**VIN\_ON (0x35)**

Description: Input voltage must be above this level before the output can be enabled.

Bit	Description	Format	Unit
15:0	Sets the VIN ON threshold in 0.25 V steps in the range 5.5 - 15 V.	Linear	V

**VIN\_OFF (0x36)**

Description: Sets the value of the PVIN input voltage, in Volts, at which the unit should stop power conversion.

Bit	Description	Format	Unit
15:0	Sets the VIN OFF threshold in 0.25 V steps. The specified range is 2.25 - 18.25 V.	Linear	V

**INTERLEAVE (0x37)**

Description: Configures the phase offset with respect to a common SYNC clock.

Bit	Function	Description	Format
11:8	Group ID Number	Value 0-15. Sets an ID number to a group of interleaved rails.	Integer Unsigned
7:4	Number in Group	Value 1 to 4. Sets the number of phases positions and the phase shift for each value of ORDER.	Integer Unsigned
3:0	Order within the group	Value 0 to NUM_GROUP - 1. Each value of ORDER adds a phase shift equal to $360^\circ / \text{NUM\_GROUP}$ .	Integer Unsigned

**IOUT\_CAL\_GAIN (0x38)**

Description: Sets the current sense resistance.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for current sensing at +25°C.	Linear	mΩ

**IOUT\_CAL\_OFFSET (0x39)**

Addressing: Phase

Description: Sets the current-sense offset.

Bit	Description	Format	Unit
15:0	Sets an offset to IOUT readings. Use to compensate for delayed measurements of current ramp.	Linear	A

**VOUT\_OV\_FAULT\_LIMIT (0x40)**

Description: Sets the overvoltage fault threshold relative to the current VOUT\_COMMAND.

Bit	Description	Format	Unit
-----	-------------	--------	------

15:0	Sets the VOUT overvoltage fault threshold, which is a fixed percentage of the current output voltage target.	Vout Mode Unsigned (Exp = -9)	* Vout
------	--	-------------------------------	--------

**VOUT\_OV\_FAULT\_RESPONSE (0x41)**

Description: Sets the VOUT OV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			10	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output overvoltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

**VOUT\_OV\_WARN\_LIMIT (0x42)**

Description: Sets the overvoltage warning threshold relative to the current VOUT\_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage warning threshold, which is a fixed percentage of the current output voltage target.	Vout Mode Unsigned (Exp = -9)	* Vout

**VOUT\_UV\_WARN\_LIMIT (0x43)**

Description: Sets the undervoltage warning threshold relative to the current VOUT\_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage warning threshold, which is a fixed percentage of the current output voltage target.	Vout Mode Unsigned (Exp = -9)	* Vout

**VOUT\_UV\_FAULT\_LIMIT (0x44)**

Description: Sets the undervoltage fault threshold relative to the current VOUT\_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage fault threshold, which is a fixed percentage of the current output voltage target.	Vout Mode Unsigned (Exp = -9)	* Vout

**VOUT\_UV\_FAULT\_RESPONSE (0x45)**

Description: Sets the VOUT UV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			10	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output undervoltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

**IOUT\_OC\_FAULT\_LIMIT (0x46)**

Addressing: Phase

Description: Sets the output over-current peak limit for per phase.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak fault threshold for each phase with PHASE command set to 0x00 - 0x03. Sets the IOUT overcurrent peak fault threshold for all phases with PHASE command set to 0xFF. The analog hardware supports values from 8 A to 62 A in 2 A steps. Adjustable range from 0-62A. Linear format with LSB=0.25A. Note that the effective current limit of the multi-phase stack is equal to the lowest IOUT_OC_FAULT_LIMIT setting times the number of phases in the stack.	Linear	A

**IOUT\_OC\_FAULT\_RESPONSE (0x47)**

Description: Sets the output total over-current fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			10	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			11	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output overcurrent delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

**IOUT\_OC\_WARN\_LIMIT (0x4A)**

Addressing: Phase

Description: Sets the value of the output current that causes the overcurrent detector to indicate an overcurrent warning condition. IOUT\_OC\_WARN\_LIMIT is a phased command. Each phase will report an output current overcurrent warning independently.

Bit	Description	Format	Unit
15:0	Sets the value of the overcurrent warning threshold for each phase with PHASE command set to 0x00 - 0x03. The analog hardware supports values from 8 A to 62 A in 2 A steps. Adjustable range from 0-62A. Linear format with LSB=0.25A.	Linear	A

**OT\_FAULT\_LIMIT (0x4F)**

Addressing: Phase

Description: Sets the over-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature fault threshold. Adjustable range from 0-160°C in 1°C steps. Setting 255°C value will disable the over-temperature fault limit without disabling the on-die Bandgap thermal shutdown.	Linear	°C

**OT\_FAULT\_RESPONSE (0x50)**

Description: Sets the over-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable, Resume When OK	The device shuts down (disables the output) until the temperature is below the over-temperature warn limit, then restarts according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.

2:0	Retry Time and Delay Time	Sets the over-temperature delay time for respond after delay and HICCUP.	0	10 ms	Shutdown delay of 10 ms, HICCUP equal to TON_RISE, HICCUP delay equal to TON_RISE.
			1	1 ms	
			2	2 ms	
			3	3 ms	
			4	4 ms	
			5	5 ms	
			6	6 ms	
			7	7 ms	

**OT\_WARN\_LIMIT (0x51)**

Addressing: Phase

Description: Sets the over-temperature warn limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature warning threshold. Adjustable range from 0-160°C in 1°C steps. Setting 255°C value will disable the OT_WARN_LIMIT function.	Linear	°C

**VIN\_OV\_FAULT\_LIMIT (0x55)**

Description: Sets the input over-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage fault threshold. Values 4 - 20 V in 1 V steps.	Linear	V

**VIN\_OV\_FAULT\_RESPONSE (0x56)**

Description: Sets the input over-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output over-voltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.

			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

**VIN\_UV\_WARN\_LIMIT (0x58)**

Addressing: Phase

Description: Sets the input under-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage warning threshold.	Linear	V

**TON\_DELAY (0x60)**

Description: Sets the turn-on delay time

Bit	Description	Format	Unit
15:0	Sets the time, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.	Linear	ms

**TON\_RISE (0x61)**

Description: Sets the turn-on ramp-up time.

Bit	Description	Format	Unit
15:0	Sets the rise time of VOUT after ENABLE and On Delay. The time can range from 0 ms to 31.75 ms in 0.25 ms steps. Values less than 0.5 ms are supported as 0.5 ms.	Linear	ms

**TON\_MAX\_FAULT\_LIMIT (0x62)**

Description: Sets an upper limit on how long the unit can attempt to power up the output without reaching the target voltage.

Bit	Description	Format	Unit
15:0	Sets the upper limit time. The time can range from 0 ms to 127 ms in 0.5 ms steps. Value 0 ms disables the TON_MAX functionality.	Linear	ms

**TON\_MAX\_FAULT\_RESPONSE (0x63)**

Description: Instructs the device on what action to take in response to TON\_MAX fault.

Bit	Function	Description	Value	Function	Description
-----	----------	-------------	-------	----------	-------------

7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output over-voltage delay time for respond after delay and HICCUP.	0	1 ms	Shutdown delay of 1 ms, HICCUP equal to TON_RISE.
			1	1 ms	Shutdown delay of 1 ms, HICCUP equal to 1 times TON_RISE.
			2	2 ms	Shutdown delay of 2 ms, HICCUP equal to 2 times TON_RISE.
			3	3 ms	Shutdown delay of 3 ms, HICCUP equal to 3 times TON_RISE.
			4	4 ms	Shutdown delay of 4 ms, HICCUP equal to 4 times TON_RISE.
			5	5 ms	Shutdown delay of 5 ms, HICCUP equal to 5 times TON_RISE.
			6	6 ms	Shutdown delay of 6 ms, HICCUP equal to 6 times TON_RISE.
			7	7 ms	Shutdown delay of 7 ms, HICCUP equal to 7 times TON_RISE.

**TOFF\_DELAY (0x64)**

Description: Sets the turn-off delay.

Bit	Description	Format	Unit
15:0	Sets the delay time from DISABLE to start of the fall of the output voltage. Normally the time can range from 0 ms up to 127.5 ms in 0.5 ms steps. An internal delay of up to 50 $\mu$ s will be added to TOFF_DELAY, even if TOFF_DELAY is equal to 0 ms.	Linear	ms

**TOFF\_FALL (0x65)**

Description: Sets the turn-off ramp-down time.

Bit	Description	Format	Unit
15:0	Sets the fall time for VOUT after DISABLE and Off Delay. The time can range from 0 ms to 31.75 ms in 0.25 ms steps. Values less than 0.5 ms will be implemented as 0.5 ms.	Linear	ms

**STATUS\_BYTE (0x78)**

Addressing: Phase

Description: Returns a brief fault/warning status byte. Setting and clearing of supported bits must be done in the individual status registers. For example, Clearing VOUT\_OVF in STATUS\_VOUT also clears VOUT\_OV in STATUS\_BYTE.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shut down due to fault.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault

**STATUS\_WORD (0x79)**

Addressing: Phase

Description: Returns an extended fault/warning status byte. Writing 0080h to STATUS\_WORD will clear the BUSY bit, if set. Writing 0180h to STATUS\_WORD will clear both the BUSY bit and UNKNOWN bit, if set.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout	An output current fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	An other fault has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shut down due to fault.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.
			1	Fault.
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No Fault.
			1	Fault.

2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.

**STATUS\_VOUT (0x7A)**

Description: Returns Vout-related fault/warning status bits. All supported bits can be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_VOUT (0x7A) register in their position.

Bit	Function	Description	Value	Description
7	Vout OV Fault	Latched flag of Vout over-voltage fault has occurred .	0	No Fault.
			1	Fault.
6	Vout OV Warn	Latched flag of Vout over-voltage warning has occurred .	0	No Fault.
			1	Fault.
5	Vout UV Warn	Latched flag of Vout under-voltage warning has occurred .	0	No Fault.
			1	Fault.
4	Vout UV Fault	Latched flag of Vout under-voltage fault has occurred .	0	No Fault.
			1	Fault.
3	Vout Min/Max Fault	Latched flag of Vout min/max fault or warning has occurred .	0	No Fault.
			1	Fault.
2	Ton Max Fault	Latched flag of Ton max fault or warning has occurred .	0	No Fault.
			1	Fault.

**STATUS\_IOUT (0x7B)**

Addressing: Phase

Description: Returns Iout-related fault/warning status bits. All supported bits can be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_IOUT (0x7B) register in their position.

Bit	Function	Description	Value	Description
7	Iout OC Fault	Latched flag of Iout over-current fault has occurred.	0	No Fault.
			1	Fault.
5	Iout OC Warn	Latched flag of Iout over-current warning has occurred.	0	No Fault.
			1	Fault.
4	Iout UC Fault	Latched flag of Iout under-current fault has occurred.	0	No Fault.
			1	Fault.
3	Current Share Fault	Latched flag of current share fault has occurred.	0	No Fault.
			1	Fault.

**STATUS\_INPUT (0x7C)**

Addressing: Phase

Description: Returns VIN/IIN-related fault/warning status bits. All supported bits can be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_INPUT register (0x7C) in their position.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Latched flag of input over-voltage fault has occurred.	0	No Fault.
			1	Fault.
6	Vin OV Warn	Latched flag of input over-voltage warning has occurred.	0	No Fault.
			1	Fault.
5	Vin UV Warn	Latched flag of input under-voltage warning has occurred.	0	No Fault.
			1	Fault.
4	Vin UV Fault	Latched flag of input under-voltage fault has occurred.	0	No Fault.
			1	Fault.
3	Low Vin Fault	Latched flag of shutdown unit due to insufficient VIN .	0	No Fault.
			1	Fault.
2	Iin Oc Fault		0	No Fault.

		Latched flag of input over-current fault has occurred.	1	Fault.
1	lin Oc Warn	Latched flag of input over-current warning has occurred.	0	No Fault.
			1	Fault.
0	Pin Op Warn	Latched flag of input over-power warning has occurred.	0	No Fault.
			1	Fault.

**STATUS\_TEMPERATURE (0x7D)**

Addressing: Phase

Description: Returns the temperature-related fault/warning status bits. All supported bits can be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_TEMPERATURE (0x7D) register in their position.

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Latched flag of over-temperature fault has occurred.	0	No Fault.
			1	Fault.
6	Overtemperature Warn	Latched flag of over-temperature warn has occurred.	0	No Fault.
			1	Fault.

**STATUS\_CML (0x7E)**

Addressing: Phase

Description: Returns Communication/Logic/Memory-related fault/warning status bits. All supported bits can be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_CML (0x7E) register in their position.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check (PEC) Failed.	0	No Failure.
			1	Failure.
4	Memory Error	A memory error was detected.	0	No Fault.
			1	Fault.
1	Other Communication Fault	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.	0	No Fault.
			1	Fault.

**STATUS\_OTHER (0x7F)**

Description: Returns one data byte with information not specified in the other STATUS\_BYTE.

Bit	Description	Value	Description
0	The device was the first to assert SMBALERT.	1	First to assert SMBALERT.
		0	The device was not the first to assert SMBALERT. This could mean either that the SMBALERT signal is not asserted (or has since been cleared), or that it is asserted, but this device was not the first on the bus to assert it.

**STATUS\_MFR\_SPECIFIC (0x80)**

Addressing: Phase

Description: Returns manufacturer specific status information. All supported bits may be cleared either by CLEAR\_FAULTS, or individually by writing 1b to the STATUS\_MFR\_SPECIFIC (0x80) register in their position.

Bit	Function	Description	Value	Description
7	Power-On Reset Fault	Power-on reset fault has occurred.	0	No Fault.
			1	Fault.
6	Power-On Self-Check	Showing the status of the Power-On Self-Check.	0	Power On Self-Check is complete. All expected BCX slaves have responded.
			1	Power-On Self-Check is in progress. One or more BCX slaves have not responded.
3	Reset	VOUT_COMMAND has been reset without PMBus commands.	0	RESET_VOUT event has not occurred.
			1	RESET_VOUT event has occurred.
2	BCX fault	Back-channel communications fault has occurred.	0	No Fault.
			1	Fault.
1	Sync fault	Sync fault has occurred.	0	No Fault.
			1	Fault.

**READ\_VIN (0x88)**

Addressing: Phase

Description: Returns the measured input voltage.

Bit	Description	Format	Unit
15:0	Returns the input voltage reading. When PHASE = FFh, READ_VIN returns the input voltage of the master device.	Linear	V

**READ\_VOUT (0x8B)**

Addressing: Phase

Description: Returns the measured output voltage.

Bit	Description	Format	Unit
15:0	Returns the output voltage reading.	Vout Mode Unsigned (Exp = -9)	V

**READ\_IOUT (0x8C)**

Addressing: Phase

Description: Returns the measured output current.

Bit	Description	Format	Unit
15:0	Returns the output current reading. When PHASE = FFh, READ_IOUT returns the total current for the stack of devices.	Linear	A

**READ\_TEMPERATURE\_1 (0x8D)**

Addressing: Phase

Description: Returns the maximum power stage temperature.

Bit	Description	Format	Unit
15:0	When PHASE = FFh, READ_TEMPERATURE_1 returns the temperature of the hottest of device in the stack of devices.	Linear	°C

**PMBUS\_REVISION (0x98)**

Description: Returns the PMBus revision number for this device.

Bit	Function	Description	Value	Function	Description
7:4	Part I Revision	Part I Revision.	0011	1.3	Part I Revision 1.3.
3:0	Part II Revision	Part II Revision.	0011	1.3	Part II Revision 1.3.

**MFR\_ID (0x99)**

Description: Sets the manufacturer ID String.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

**MFR\_MODEL (0x9A)**

Description: Sets the manufacturer model string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

**MFR\_REVISION (0x9B)**

Description: Sets the manufacturer revision string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

**MFR\_SERIAL (0x9E)**

Description: Sets the manufacturer serial number.

Bit	Description	Format
23:0	3-byte serial number assigned by manufacturer.	Byte Array

**IC\_DEVICE\_ID (0xAD)**

Description: Reports identification information.

Bit	Description	Format
47:0	Reports identification information.	Byte Array

**IC\_DEVICE\_REV (0xAE)**

Description: Reports revision information.

Bit	Description	Format
15:0	Reports revision information.	Byte Array

**USER\_DATA\_01 (0xB1)**

Addressing: Phase

Description: Configures the control loop compensation settings.

Bit	Function	Description	Format
39:38	SEL_CZI High	High bits component of CZI scalar.	Byte Array
25:24	SEL_CZI Low	Low bits component of CZI scalar.	Byte Array

23:22	SEL_CZV High	High bits component of CZV scalar.	Byte Array
9:8	SEL_CZV Low	Low bits component of CZV scalar.	Byte Array

Bit	Function	Description	Value	Function	Description
37:33	CPI	Selects the value of current loop filter capacitor.	00000	0 pF	
			00001	3.2 pF	
			00010	6.4 pF	
			00011	9.6 pF	
			00100	12.8 pF	
			00101	16 pF	
			00110	19.2 pF	
			00111	22.4 pF	
			01000	25.6 pF	
			01001	28.8 pF	
			01010	32 pF	
			01011	35.2 pF	
			01100	38.4 pF	
			01101	41.6 pF	
			01110	44.8 pF	
			01111	48 pF	
			10000	51.2 pF	
			10001	54.4 pF	
			10010	57.6 pF	
			10011	60.8 pF	
32	CZI multiplier	Selects the value of current loop integrating capacitor multiplier.	0	1	
			1	2	
31:26	RVI	Selects the value of current loop mid-band gain resistor.	000000	0 kΩ	
			000001	5 kΩ	
			000010	10 kΩ	
			000011	15 kΩ	
			000100	20 kΩ	
			000101	25 kΩ	
			000110	30 kΩ	
			000111	35 kΩ	
			001000	40 kΩ	
			001001	45 kΩ	
			001010	50 kΩ	
			001011	55 kΩ	
			001100	60 kΩ	
			001101	65 kΩ	
001110	70 kΩ				
001111	75 kΩ				

			010000	80 kΩ	
			010001	85 kΩ	
			010010	90 kΩ	
			010011	95 kΩ	
			010100	100 kΩ	
			010101	105 kΩ	
			010110	110 kΩ	
			010111	115 kΩ	
			011000	120 kΩ	
			011001	125 kΩ	
			011010	130 kΩ	
			011011	135 kΩ	
			011100	140 kΩ	
			011101	145 kΩ	
			011110	150 kΩ	
			011111	155 kΩ	
			100000	160 kΩ	
			100001	165 kΩ	
			100010	170 kΩ	
			100011	175 kΩ	
			100100	180 kΩ	
			100101	185 kΩ	
			100110	190 kΩ	
			100111	195 kΩ	
			101000	200 kΩ	
			101001	205 kΩ	
			101010	210 kΩ	
			101011	215 kΩ	
			101100	220 kΩ	
			101101	225 kΩ	
			101110	230 kΩ	
			101111	235 kΩ	
			110000	240 kΩ	
			110001	245 kΩ	
			110010	250 kΩ	
			110011	255 kΩ	
			110100	260 kΩ	
			110101	265 kΩ	
			110110	270 kΩ	
			110111	275 kΩ	
			111000	280 kΩ	
			111001	285 kΩ	
			111010	290 kΩ	
			111011	295 kΩ	
			111100	300 kΩ	
			111101	305 kΩ	
			111110	310 kΩ	
			111111	315 kΩ	
21:17	CPV	Selects the value of voltage loop filter capacitor.	00000	0 pF	
			00001	6.25 pF	
			00010	12.5 pF	
			00011	18.75 pF	
			00100	25 pF	
			00101	31.25 pF	
			00110	37.5 pF	

			00111	43.75 pF	
			01000	50 pF	
			01001	56.25 pF	
			01010	62.5 pF	
			01011	68.75 pF	
			01100	75 pF	
			01101	81.25 pF	
			01110	87.5 pF	
			01111	93.75 pF	
			10000	100 pF	
			10001	106.25 pF	
			10010	112.5 pF	
			10011	118.75 pF	
			10100	125 pF	
			10101	131.25 pF	
			10110	137.5 pF	
			10111	143.75 pF	
			11000	150 pF	
			11001	156.25 pF	
			11010	162.5 pF	
			11011	168.75 pF	
			11100	175 pF	
			11101	181.25 pF	
			11110	187.5 pF	
			11111	193.75 pF	
15:10	RVV	Selects the value of voltage loop mid-band gain resistor.	000000	0 kΩ	
			000001	5 kΩ	
			000010	10 kΩ	
			000011	15 kΩ	
			000100	20 kΩ	
			000101	25 kΩ	
			000110	30 kΩ	
			000111	35 kΩ	
			001000	40 kΩ	
			001001	45 kΩ	
			001010	50 kΩ	
			001011	55 kΩ	
			001100	60 kΩ	
			001101	65 kΩ	
			001110	70 kΩ	
			001111	75 kΩ	
			010000	80 kΩ	
			010001	85 kΩ	
			010010	90 kΩ	
			010011	95 kΩ	
			010100	100 kΩ	
			010101	105 kΩ	
			010110	110 kΩ	
			010111	115 kΩ	
			011000	120 kΩ	
			011001	125 kΩ	
			011010	130 kΩ	
			011011	135 kΩ	
			011100	140 kΩ	
			011101	145 kΩ	

			011110	150 kΩ	
			011111	155 kΩ	
			100000	160 kΩ	
			100001	165 kΩ	
			100010	170 kΩ	
			100011	175 kΩ	
			100100	180 kΩ	
			100101	185 kΩ	
			100110	190 kΩ	
			100111	195 kΩ	
			101000	200 kΩ	
			101001	205 kΩ	
			101010	210 kΩ	
			101011	215 kΩ	
			101100	220 kΩ	
			101101	225 kΩ	
			101110	230 kΩ	
			101111	235 kΩ	
			110000	240 kΩ	
			110001	245 kΩ	
			110010	250 kΩ	
			110011	255 kΩ	
			110100	260 kΩ	
			110101	265 kΩ	
			110110	270 kΩ	
			110111	275 kΩ	
			111000	280 kΩ	
			111001	285 kΩ	
			111010	290 kΩ	
			111011	295 kΩ	
			111100	300 kΩ	
			111101	305 kΩ	
			111110	310 kΩ	
			111111	315 kΩ	
5:4	GMV	Selects the value of voltage error transconductance.	00	25 μS	
			01	50 μS	
			10	100 μS	
			11	200 μS	
1:0	GMI	Selects the value of current error transconductance.	00	25 μS	
			01	50 μS	
			10	100 μS	
			11	200 μS	

**TELEMETRY\_CONFIG (0xD0)**

Description: Configures the priority and averaging for each channel of the internal telemetry system. The internal telemetry system shares a single ADC across each measurement. The priority setting allows the user to adjust the relative rate of measurement of each telemetry value. The ADC will first measure each value with a priority A value. With each pass through all priority A measurements, one priority B measurement will be taken. With each pass through all priority B measurements, one priority C measurement will be taken.

Bit	Function	Description	Value	Function	Description
31:30	READ_VIN Priority	Assigns priority A-C to input voltage telemetry.	00	A priority	
			01	B priority	
			10	C priority	

			11	Disable input voltage telemetry.	
26:24	READ_VIN Rolling Avg	READ_VIN Rolling average of $2^N$ samples.	000	1 sample (N=0)	
			001	2 samples (N=1)	
			010	4 samples (N=2)	
			011	8 samples (N=3)	
			100	16 samples (N=4)	
			101	32 samples (N=5)	
23:22	READ_TEMPERATURE_1 Priority	Assigns priority A-C to output temperature telemetry. The temperature telemetry cannot be disabled because it is used for Over-temperature Protection.	00	A priority	
			01	B priority	
			10	C priority	
18:16	READ_TEMPERATURE_1 Rolling Avg	READ_TEMPERATURE_1 Rolling average of $2^N$ samples.	000	1 sample (N=0)	
			001	2 samples (N=1)	
			010	4 samples (N=2)	
			011	8 samples (N=3)	
			100	16 samples (N=4)	
			101	32 samples (N=5)	
15:14	READ_IOUT Priority	Assigns priority A-C to output current telemetry.	00	A priority	
			01	B priority	
			10	C priority	
			11	Disable output current telemetry.	
10:8	READ_IOUT Rolling Avg	READ_IOUT Rolling average of $2^N$ samples.	000	1 sample (N=0)	
			001	2 samples (N=1)	
			010	4 samples (N=2)	
			011	8 samples (N=3)	
			100	16 samples (N=4)	
			101	32 samples (N=5)	
7:6	READ_VOUT Priority	Assigns priority A-C to output voltage telemetry.	00	A priority	
			01	B priority	
			10	C priority	

			11	Disable output voltage telemetry.	
2:0	READ_VOUT Rolling Avg	READ_VOUT Rolling average of 2 <sup>N</sup> samples.	000	1 sample (N=0)	
			001	2 samples (N=1)	
			010	4 samples (N=2)	
			011	8 samples (N=3)	
			100	16 samples (N=4)	
			101	32 samples (N=5)	

**READ\_ALL (0xDA)**

Description: Returns a 14-byte block of STATUS\_WORD and telemetry values. This can reduce bus utilization by combining multiple read functions into a single command.

Bit	Function	Description	Format	Unit
79:64	Read Vin	Returns the input voltage reading. When PHASE = FFh, READ_VIN returns the input voltage of the master device.	Linear	V
63:48	Read Temperature 1	When PHASE = FFh, READ_TEMPERATURE_1 returns the temperature of the hottest of device in the stack of devices.	Linear	°C
47:32	Read Iout	Returns the output current reading. When PHASE = FFh, READ_IOUT returns the total current for the stack of devices.	Linear	A
31:16	Read Vout	Returns the output voltage reading.	Vout Mode Unsigned (Exp = -9)	V

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout	An output current fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	An other fault has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shut down due to fault.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4		An output overcurrent fault has occurred.	0	No Fault.

	Iout Overcurrent Fault		1	Fault.
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.

**STATUS\_ALL (0xDB)**

Description: Returns 7-byte block of STATUS command codes. This can reduce bus utilization to read multiple faults.

Bit	Function	Description	Value	Description
55	Power-On Reset Fault	Power-on reset fault has occurred.	0	No Fault.
			1	Fault.
54	Power-On Self-Check	Showing the status of the Power-On Self-Check.	0	Power On Self-Check is complete. All expected BCX slaves have responded.
			1	Power-On Self-Check is in progress. One or more BCX slaves have not responded.
51	Reset	VOUT_COMMAND has been reset without PMBus commands.	0	RESET_VOUT event has not occurred.
			1	RESET_VOUT event has occurred.
50	BCX fault	Back-channel communications fault has occurred.	0	No Fault.
			1	Fault.
49	Sync fault	Sync fault has occurred.	0	No Fault.
			1	Fault.
40	First to Alert	The device was the first to assert SMBALERT.	1	First to assert SMBALERT.
			0	The device was not the first to assert SMBALERT. This could mean either that the SMBALERT signal is not asserted (or has since been cleared), or that it is asserted, but this device was not the first on the bus to assert it.
39	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
38	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
37	Packet Error Check Failed	Packet Error Check (PEC) Failed.	0	No Failure.
			1	Failure.
36	Memory Error	A memory error was detected.	0	No Fault.
			1	Fault.
33			0	No Fault.

	Other Communication Fault	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.	1	Fault.
31	Overtemperature Fault	Latched flag of over-temperature fault has occurred.	0	No Fault.
			1	Fault.
30	Overtemperature Warn	Latched flag of over-temperature warn has occurred.	0	No Fault.
			1	Fault.
23	Vin Overvoltage Fault	Latched flag of input over-voltage fault has occurred.	0	No Fault.
			1	Fault.
22	Vin OV Warn	Latched flag of input over-voltage warning has occurred.	0	No Fault.
			1	Fault.
21	Vin UV Warn	Latched flag of input under-voltage warning has occurred.	0	No Fault.
			1	Fault.
20	Vin UV Fault	Latched flag of input under-voltage fault has occurred.	0	No Fault.
			1	Fault.
19	Low Vin Fault	Latched flag of shutdown unit due to insufficient VIN .	0	No Fault.
			1	Fault.
18	Iin Oc Fault	Latched flag of input over-current fault has occurred.	0	No Fault.
			1	Fault.
17	Iin Oc Warn	Latched flag of input over-current warning has occurred.	0	No Fault.
			1	Fault.
16	Pin Op Warn	Latched flag of input over-power warning has occurred.	0	No Fault.
			1	Fault.
15	Iout OC Fault	Latched flag of Iout over-current fault has occurred.	0	No Fault.
			1	Fault.
13	Iout OC Warn	Latched flag of Iout over-current warning has occurred.	0	No Fault.
			1	Fault.
12	Iout UC Fault	Latched flag of Iout under-current fault has occurred.	0	No Fault.
			1	Fault.
11	Current Share Fault	Latched flag of current share fault has occurred.	0	No Fault.
			1	Fault.
7	Vout OV Fault	Latched flag of Vout over-voltage fault has occurred .	0	No Fault.
			1	Fault.
6	Vout OV Warn	Latched flag of Vout over-voltage warning has occurred .	0	No Fault.
			1	Fault.
5	Vout UV Warn	Latched flag of Vout under-voltage warning has occurred .	0	No Fault.
			1	Fault.
4	Vout UV Fault	Latched flag of Vout under-voltage fault has occurred .	0	No Fault.
			1	Fault.
3	Vout Min/Max Fault	Latched flag of Vout min/max fault or warning has occurred .	0	No Fault.
			1	Fault.
2	Ton Max Fault	Latched flag of Ton max fault or warning has occurred .	0	No Fault.
			1	Fault.

**STATUS\_PHASE (0xDC)**

Addressing: Phase

Description: When PHASE = FFh or 80h, reads to this command return a data word detailing which phases have experienced fault conditions. When PHASE != FFh, reads to this command return a data word detailing which fault(s) the current PHASE has experienced. PHASE number assignment is per PHASE\_CONFIG.

Bit	Function	Description	Value	Description
3	Phase 4 Fault		0	

		The module assigned to PHASE=3 has experienced a fault. Set PHASE = 3, and read STATUS_WORD or STATUS_ALL for more information.	1	
2	Phase 3 Fault	The module assigned to PHASE=2 has experienced a fault. Set PHASE = 2, and read STATUS_WORD or STATUS_ALL for more information.	0	
			1	
1	Phase 2 Fault	The module assigned to PHASE=1 has experienced a fault. Set PHASE = 1, and read STATUS_WORD or STATUS_ALL for more information.	0	
			1	
0	Phase 1 Fault	The module assigned to PHASE=0 has experienced a fault. Set PHASE = 0, and read STATUS_WORD or STATUS_ALL for more information.	0	
			1	

**PGOOD\_CONFIG (0xE3)**

Description: Provides control of the delays asserting and releasing PGOOD.

Bit	Function	Description	Value	Function	Description
15:12	PGOOD Off Delay	Sets Delay from the detection of an unmasked Fault or Warning event to the assertion of PGOOD low. 0d: Delay PGOOD high-low: 1 PWM CLK 1d-15d: Delay PGOOD high-low: 2 <sup>N</sup> +1 PWM CLKs	0x0	1 PWM CLK	
			0x1	3 PWM CLKs	
			0x2	5 PWM CLKs	
			0x3	9 PWM CLKs	
			0x4	17 PWM CLKs	
			0x5	33 PWM CLKs	
			0x6	65 PWM CLKs	
			0x7	129 PWM CLKs	
			0x8	257 PWM CLKs	
			0x9	513 PWM CLKs	
			0xA	1025 PWM CLKs	
			0xB	2049 PWM CLKs	
			0xC	4097 PWM CLKs	
			0xD	8193 PWM CLKs	
			0xE	16385 PWM CLKs	
			0xF	32769 PWM CLKs	
11:8	PGOOD On Delay	Sets Delay from the detection of no unmasked Fault or Warning events to the release of PGOOD low. 0d: Delay PGOOD low-high: 1 PWM CLK 1d-15d: Delay PGOOD low-high: 2 <sup>N</sup> +1 PWM CLKs	0x0	1 PWM CLK	
			0x1	3 PWM CLKs	
			0x2	5 PWM CLKs	
			0x3	9 PWM CLKs	
			0x4	17 PWM CLKs	
			0x5	33 PWM CLKs	
			0x6	65 PWM CLKs	
			0x7	129 PWM CLKs	

			0x8	257 PWM CLKs	
			0x9	513 PWM CLKs	
			0xA	1025 PWM CLKs	
			0xB	2049 PWM CLKs	
			0xC	4097 PWM CLKs	
			0xD	8193 PWM CLKs	
			0xE	16385 PWM CLKs	
			0xF	32769 PWM CLKs	
7	PGOOD Output Overvoltage Fault	Controls if Output Overvoltage Fault should assert PGOOD low.	0	True	PGOOD asserted low by Output Overvoltage Fault
			1	False	PGOOD not asserted low by Output Overvoltage Fault
6	PGOOD Output Overvoltage Warning	Controls if Output Overvoltage Warning should assert PGOOD low.	0	True	PGOOD asserted low by Output Overvoltage Warning
			1	False	PGOOD not asserted low by Output Overvoltage Warning
5	PGOOD Output Undervoltage Fault	Controls if Output Undervoltage Fault should assert PGOOD low.	0	True	PGOOD asserted low by Output Undervoltage Fault
			1	False	PGOOD not asserted low by Output Undervoltage Fault
4	PGOOD Output Undervoltage Warning	Controls if Output Undervoltage Warning should assert PGOOD low.	0	True	PGOOD asserted low by Output Undervoltage Warning
			1	False	PGOOD not asserted low by Output Undervoltage Warning
3	PGOOD Output Overcurrent Warning	Controls if Output Overcurrent Warning should assert PGOOD low.	0	True	PGOOD asserted low by Output Overcurrent Warning
			1	False	PGOOD not asserted low by Output Overcurrent Warning
2	PGOOD Output Overcurrent Fault	Controls if Output Overcurrent Fault should assert PGOOD low.	0	True	PGOOD asserted low by Output Overcurrent Fault
			1	False	PGOOD not asserted low by Output Overcurrent Fault
1	PGOOD Input Overvoltage Warning	Controls if Input Overvoltage Warning should assert PGOOD low.	0	True	PGOOD asserted low by Input Overvoltage Warning
			1	False	PGOOD not asserted low by Input Overvoltage Warning
0	PGOOD Input Overvoltage Fault	Controls if Input Overvoltage Fault should assert PGOOD low.	0	True	PGOOD asserted low by Input Overvoltage Fault
			1	False	PGOOD not asserted low by Input Overvoltage Fault

#### SYNC\_CONFIG (0xE4)

Description: Configures synchronization options.

Bit	Function	Description	Value	Function	Description
-----	----------	-------------	-------	----------	-------------

7:6	Sync Dir	When SYNC_DIR = 11b - Enable Auto Detect, the SYNC_IN or SYNC_OUT will be selected based on the state of the SYNC pin when the enable Condition, as defined by ON_OFF_CONFIG is met.	00	SYNC Disabled	
			01	Sync out	
			10	Sync in	
			11	Auto Detect Sync	
5	Sync Edge	Synchronizes to falling or rising edge of SYNC.	0	Falling Edge	
			1	Rising Edge	

**STACK\_CONFIG (0xEC)**

Description: Configures multi-phase stack settings.

Bit	Function	Description	Format
7:4	BCX Start	BCX address for stack master.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
3:0	BCX Stop	Configures multi-phase stack settings.	0000	Stand Alone, 1 Phase	
			0001	1 Slave, 2 Phases	
			0010	2 Slaves, 3 Phases	
			0011	3 Slaves, 4 Phases	

**MISC\_OPTIONS (0xED)**

Description: Configures miscellaneous settings.

Bit	Function	Description	Value	Function	Description
15	Require Packet Error Check	Enables/Disables Packet Error Check.	0		Disabled
			1		Enabled
14	Reset on Shutdown	Resets VOUT_COMMAND to VBOOT on shutdown.	0		VOUT_COMMAND will be unchanged following a shutdown.
			1		VOUT_COMMAND will be changed to VBOOT on a Control or OPERATION shutdown.
13	Reset on Fault	Resets VOUT_COMMAND to VBOOT on fault restart.	0		VOUT_COMMAND will be unchanged following a Fault Restart.
			1		VOUT_COMMAND will be changed to VBOOT on Restart from a Fault when Fault Retry is set to Retry after Fault.
12	Reset	Sets the function of the PGOOD/RESET pin.	0	PGOOD	
3	Pull-up	Sets the pull-up of the PGD/RESET_B pin when RESET# = 1b.	0	Disabled	Disabled
2	Fault Count	Fault count.	0	Counts down 1 cycle	Fault Counter counts down one cycle on PWM cycle without fault.

			1	Resets to 0	Fault Counter resets counter to 0 on PWM cycle without fault.
1:0	ADC Resolution	Sets the ADC resolution.	00	12-bit	
			01	10-bit	
			10	8-bit	
			11	6-bit	

**PIN\_DETECT\_OVERRIDE (0xEE)**

Description: Prevents the Default or User Store values from over-writing the pin-programmed value.

Bit	Function	Description	Value	Function	Description
12	STACK_CONFIG	Decides if STACK_CONFIG will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
11	SYNC_CONFIG	Decides if SYNC_CONFIG will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
9	COMPENSATION_CONFIG	Decides if COMPENSATION_CONFIG will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
8	SLAVE_ADDRESS	Decides if SLAVE_ADDRESS will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
5	INTERLEAVE	Decides if INTERLEAVE will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
3	TON_RISE	Decides if TON_RISE will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
2	IOUT_OC_FAULT/WARN_LIMIT	Decides if IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	
1	FREQUENCY_SWITCH	Decides if FREQUENCY_SWITCH will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
0	Vout Related Commands	Decides if VOUT_COMMAND, VOUT_SCALE_LOOP, VOUT_MAX, and VOUT_MIN will be restored from NVM or pin detection at power-up or RESTORE.	0	NVM	
			1	Pin Detection	

**SLAVE\_ADDRESS (0xEF)**

Description: Used to program or read-back the slave address of digital communication. When a slave address is updated, the device starts responding to the new address immediately.

Bit	Description	Format
6:0	Sets or retrieves the PMBus slave address. There are a number of slave address values which are reserved in the SMBus specification. The following reserved addresses are invalid and can not be programmed: 0x0C, 0x28, 0x37 and 0x61.	Integer Unsigned

**NVM\_CHECKSUM (0xF0)**

Description: Reports the CRC-16 (polynomial 0x8005) checksum for the current NVM settings.

Bit	Description	Format
15:0	CRC16 for EEPROM settings.	Integer Unsigned

**SIMULATE\_FAULT (0xF1)**

Description: Simulates fault and warning conditions by triggering the output of the detection circuit for that controls it. Multiple faults and/or warnings can be simulated at once.

Bit	Function	Description	Value	Description
15	Fault Persist	Persist simulated faults.	0	Simulated faults are automatically removed after one Fault response.
			1	Simulated faults persist until SIMULATE_FAULT is written again.
14	Sim Temp OTF	Simulate over-temperature fault	0	
			1	
12	Sim IOU OCF	Simulate output current over-current fault.	0	
			1	
11	Sim VIN UVLO	Simulate VIN undervoltage lockout.	0	
			1	
10	Sim VIN OVF	Simulate VIN over-voltage fault.	0	
			1	
9	Sim VOUT UVF	Simulate VOUT under-voltage fault.	0	
			1	
8	Sim VOUT OVF	Simulate VOUT over-voltage fault.	0	
			1	
7	Warn Persist	Persist simulated warnings.	0	Simulated warnings are automatically removed after one Fault response.
			1	Simulated warnings persist until SIMULATE_FAULT is written again.
4	Sim IOU OCW	Simulate output current over-current warning.	0	
			1	
3	Sim VIN UVW	Simulate VIN under-voltage warning.	0	
			1	
1	Sim VOUT UVW	Simulate VOUT under-voltage warning.	0	
			1	
0	Sim VOUT OVW	Simulate VOUT over-voltage warning.	0	
			1	

