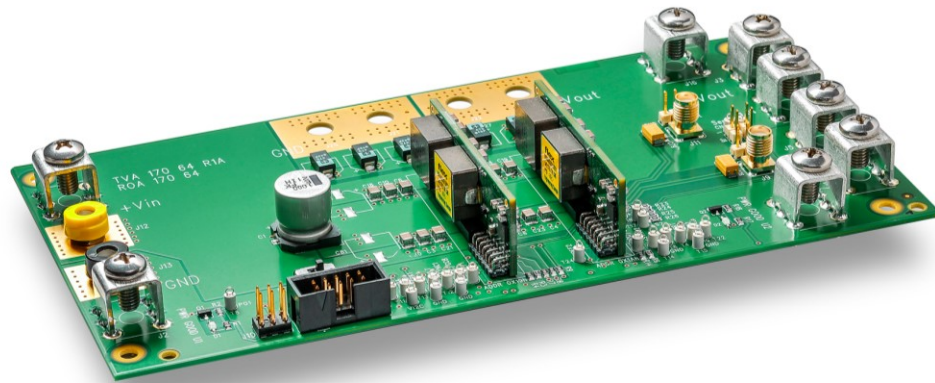


POL BMR465 Evaluation Board

ROA 170 64

User Guide



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1 Introduction

This User Guide provides a brief introduction and instruction on how to use the Reference Board ROA 170 64. This board provides the possibility to evaluate the BMR 465 / BMR 467 SIP modules either as standalone or two modules in parallel.

The User Guide also provides a description of how the layout guidelines provided in the BMR 465 / BMR 467 Technical Specification have been applied to the Reference Board layout.

1.1 Prerequisites

In order to operate the ROA 170 64 board the following is needed:

- DC power supply 7.5-14 V.
- One or more BMR 465 / BMR 467 SIP modules. Either modules or sockets can be soldered to the board. Sockets make it easy to switch between modules. Suitable sockets are for instance Mill-Max 8114-0-15-15-16-27-04-0 or Digi-Key ED90542-ND (signal header) and Mill-Max 3450-0-15-15-18-27-04-0 or Digi-Key ED1195-ND (power pins).
- USB-PMBus adapter Flex Power KEP 910 17. It is only needed when the PMBus shall be used.
- The “Flex Power Designer” software package and a compatible Windows PC. Users must be familiar with the Windows® operating system.

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2 Reference Board ROA 170 64

Power the board by connecting 7.5-14 V DC power to the “Vin” and “GND” connectors.

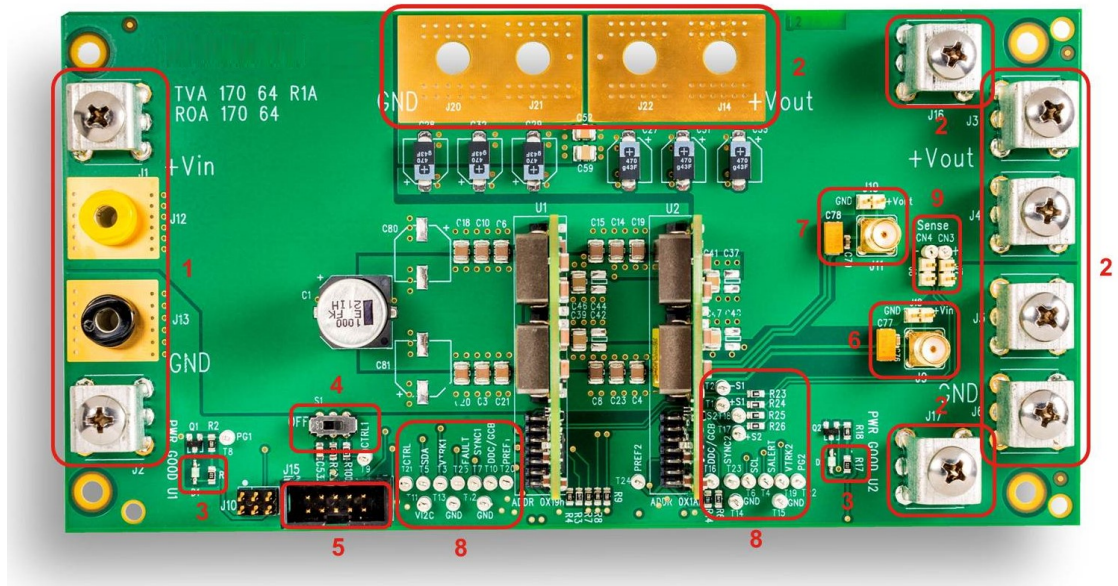


Figure 2.1 Top side of the reference board ROA 170 64.

Position Description

- 1 Input voltage connectors, +Vin/GND
- 2 Output voltage connectors, +Vout/GND
- 3 Power good LEDs, D1/D2
- 4 CONTROL switch, S1
- 5 Connector for the Flex Power KEP 910 17 USB-PMBus adapter, J15
- 6 SMA oscilloscope connector input, J9
- 7 SMA oscilloscope connector output, J11
- 8 Test points, T1-T25. Note that test point T25 is to monitor FAULT signal. This signal is available only in BMR 465.
- 9 Output voltage sense points, CN3/CN4

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3 USB-PMBus adapter

The USB-PMBus adapter used with this board is the Flex Power KEP 910 17.

3.1 Connection of Flex Power KEP 910 17 USB-PMBus adapter

Connect the Flex Power KEP 910 17 USB-PMBus adapter to the J15 header, see Figure 3.1.

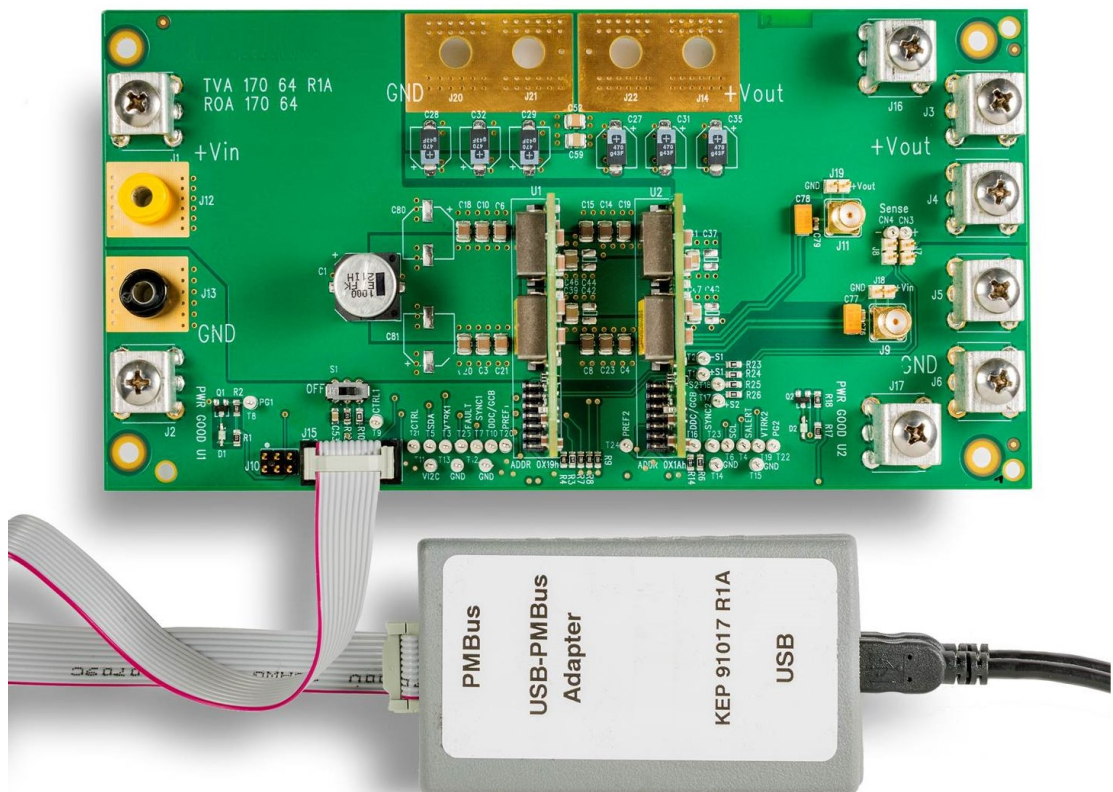


Figure 3.1 Connection of the Flex Power KEP 910 17 USB-PMBus adapter.

4 Power-up and Power-down Instructions

4.1 Power-up instruction

- The board shall be populated with one or two BMR 465 / BMR 467 SIP modules. If two modules are populated they will be operated in parallel which requires special reconfiguration using Flex Power Power Designer. If only one module is populated it is recommended to use the right position since the test points for VIN/VOUT connect to its pins.

Note: Modules operated in parallel must be of same type, thus BMR 465 and BMR 467 cannot be mixed on the same board.

- Connect the PMBus Adapter/Cable to the board.
- Connect and turn on the 7.5-14 V supply. Note that the module(s) can be started-up if enabled with input power even the PMBus adapter is not plugged-in.
- Turn the CONTROL switch S1 in On position.
- Start the software program.
- The power good LEDs for each module should now give green light. The LEDs are controlled by PG output of each BMR 465 / BMR 467 SIP module, but supplied from the USB-PMBus adapter. (For this reason the LEDs will also give green light if the USB-PMBus adapter is connected, but Vin supply is not connected or if a module position is not populated).

Note: Make sure no resistor is populated for positions R10, R21 and R22. Otherwise the modules would not start up.

4.2 Power-down instruction

- Turn the CONTROL switch in Off position or turn Off the 7.5-14 V supply or disable with PMBus.

5 VSET and address resistors

5.1 Adjustment of VSET resistors

To change the output voltage, change the resistor values as shown in Figure 5.1.

Resistors R3 and R6 can be replaced in order to change the predefined output voltage. Refer to the technical specification to select values. Note that the populated resistors give 1.8 V output.

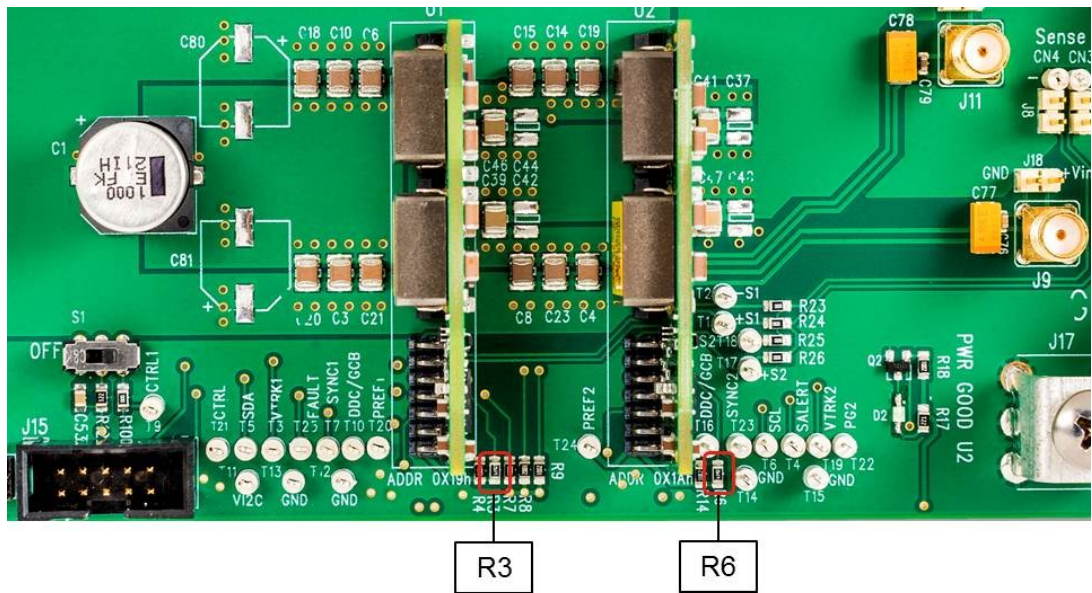


Figure 5.1 VSET resistors.

5.2 Adjustment of address resistors

To change the addresses change the resistor values as shown in Figure 5.2.

Change resistors R4 and/or R14 to achieve the desired PMBus address for the modules. Refer to chapter “PMBus addressing” in the technical specification to select the values of R4 and R14.

Note that each module must have its own unique address so a host can distinguish between the devices.

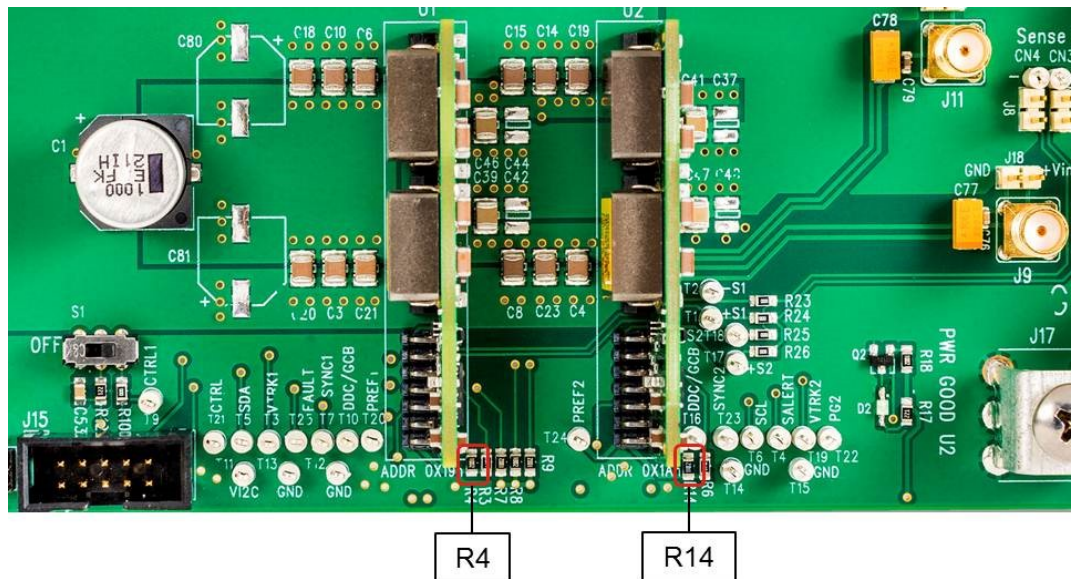


Figure 5.2 Address resistors.

6 Test Points

Input voltage should be measured at test points J18. J18/J9 and J19/J11 connect directly to the VIN/GND resp. VOUT/GND pins of the module in position U2.

CN3/CN4 connect to points close to output voltage connectors J21/J22. If J7/J8 jumpers are populated the modules will sense at the same points, but if J7, J8 is not populated the modules will use internal sense with reduced voltage accuracy.

See the schematic of the board for more information.

Test points are provided for most signals according to printing on the test board.

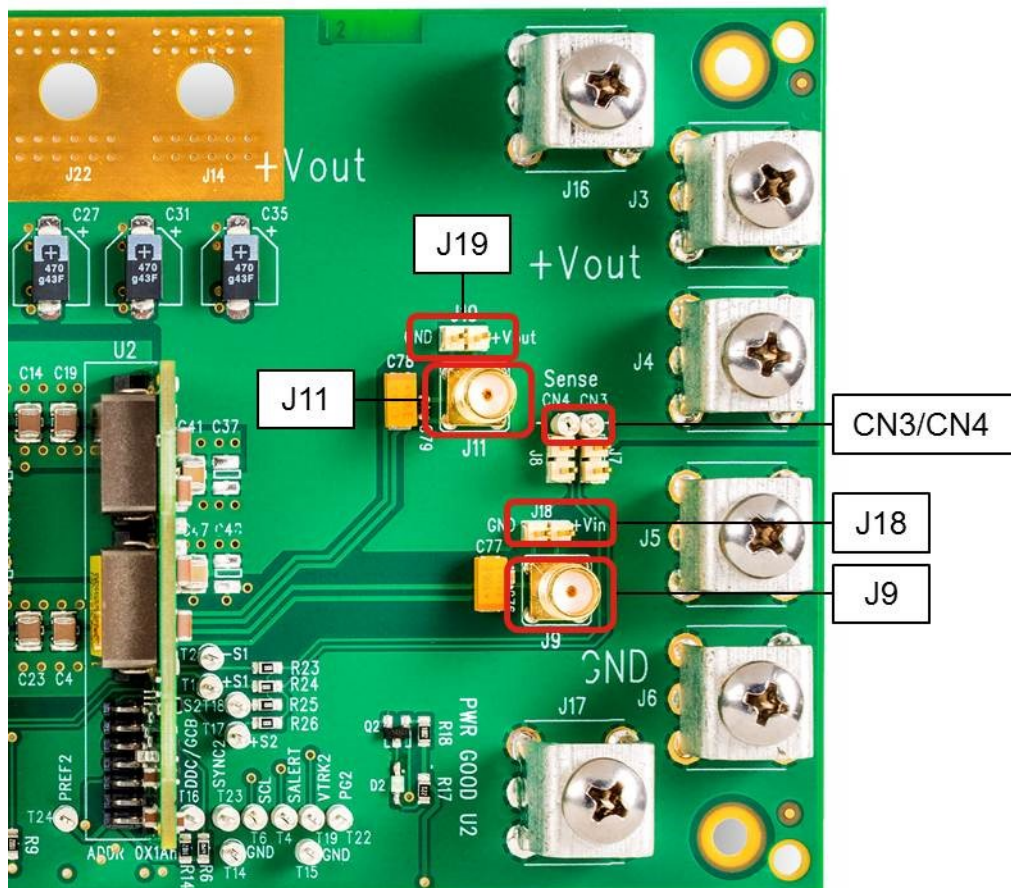


Figure 6.1 Sense points

7 Layout Description

7.1 Layout description

The following sections describe how the layout guidelines provided in the BMR 465 / BMR 467 Technical Specification have been applied to the Reference Board layout. The purpose is to give the reader a better understanding of the guidelines by examples. Please note that every system is different and that there may well be considerations to make which are not provided here, depending on the system requirements and limitations set in the end application.

7.2 PCB stack-up summary

Layer	Description	Thickness
Top layer	VIN, VOUT, GND planes Component footprints, signal traces	70 μm / 2 oz
Layer 2	GND plane Sense traces	105 μm / 3 oz
Layer 3	VIN, VOUT, GND planes	105 μm / 3 oz
Layer 4	GND plane	105 μm / 3 oz
Layer 5	VIN, VOUT, GND planes	105 μm / 3 oz
Bottom layer	GND plane Component footprints, signal traces	70 μm / 2 oz

7.3 Power pins

Refer to Figure 7.1. The power pins (VIN, VOUT and GND) should connect with low impedance to internal power planes in order to:

- Provide effective heat spread from module to the application board.
- Provide low electrical impedance to input and output capacitors, minimizing the input and output ripple levels.
- Provide a low resistance path for input and output current of the module, lowering the resistive losses.

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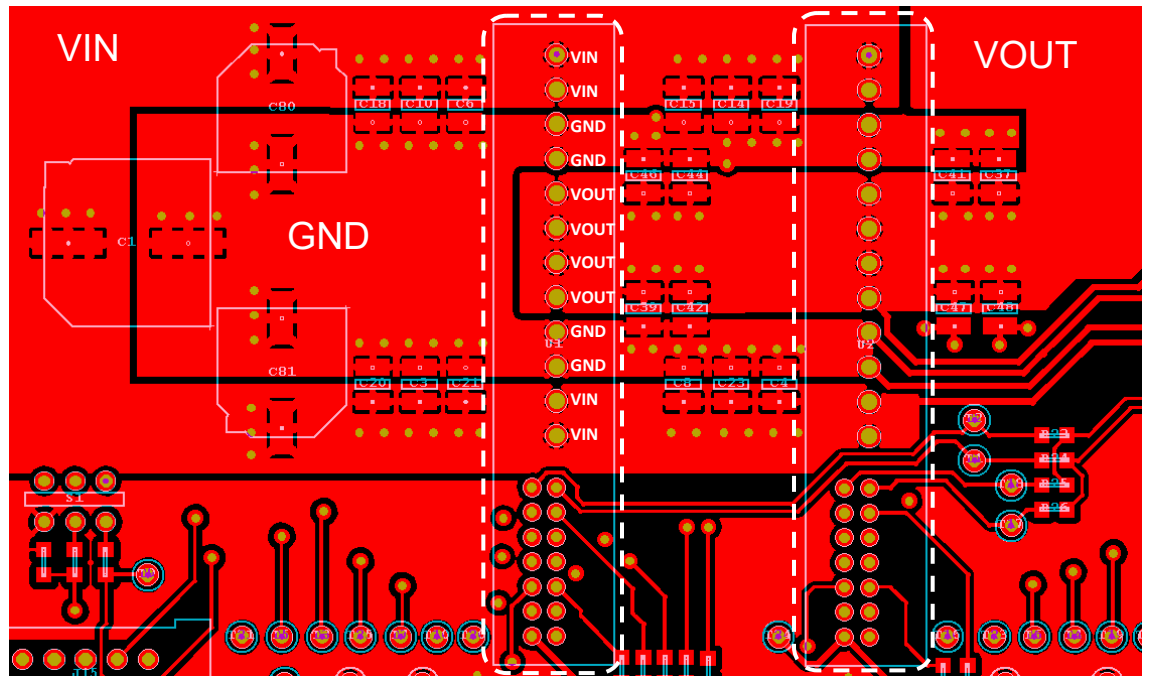


Figure 7.1. Top layer. Connection of power pins. BMR 465/BMR 467 modules in dashed areas.

This board is designed for through-hole SIP modules which means the currents are quite effectively spread to the inner layers of the PCB. In the cases where an SMD variant of the product is used it is recommended to place multiple vias around the power pads on outer layers in order to provide good path for current and heat to the inner layers (also for through hole mounted modules vias can be used to further improve current and heat transfer).

7.4 Input capacitance

Refer to Figure 7.2. The smaller ceramic input capacitors (used mainly to lower the input voltage ripple level) are placed close to the VIN/GND pins of the module in order to minimize the connection impedance. For the same reason multiple vias are placed close to the capacitors' terminals, utilizing also the inner layers to connect the capacitors to the input pins of the modules. An even better connection can be achieved by embedding the capacitor's terminals in the planes (no thermal clearance) and/or placing the vias directly in the terminal pads of the capacitors.

Note that ceramic input capacitors are also placed on the bottom side of the board, at the same locations as the ceramic capacitors shown in Figure 7.2.

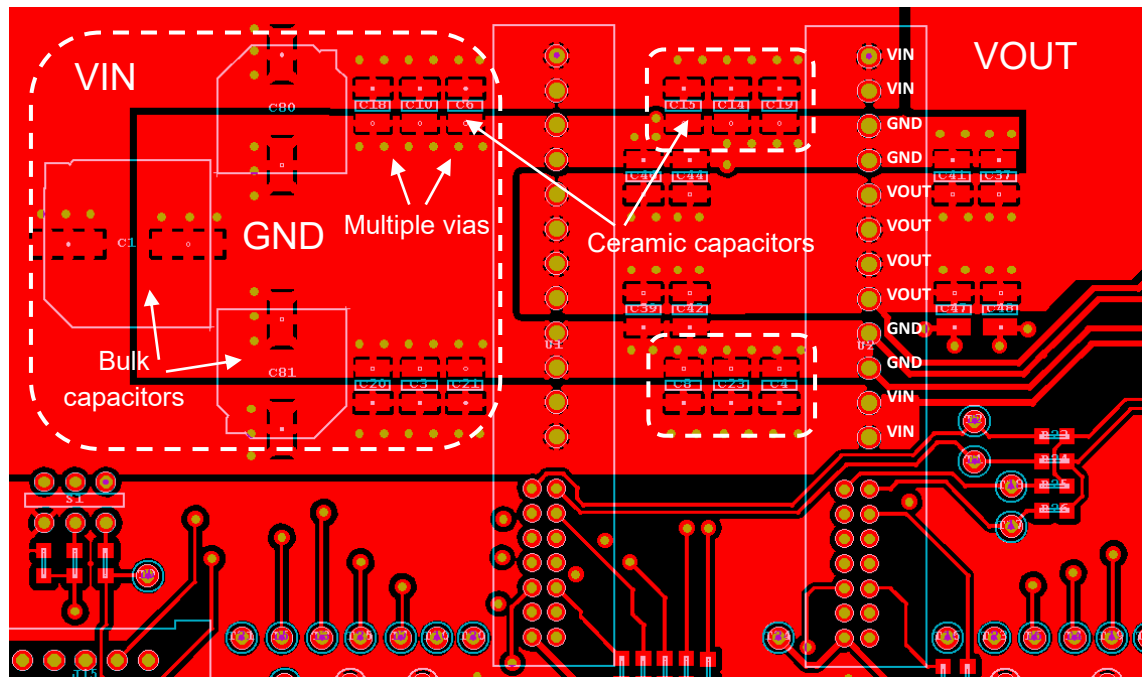


Figure 7.2. Top layer. Input capacitance in dashed areas.

Care should be taken when placing multiple vias regarding the fact that this could lead to large voids in the internal power planes, giving narrow passages for the large currents that may have to pass.

Placement and connections of the larger bulk input capacitor (used mainly to hold up the input voltage during large load transients or changes in input voltage) follows the rules of the ceramics described above. However in this case low impedance is not as critical due to the slower action, so the capacitor can be placed “behind” the ceramic input capacitors at a larger distance from the module.

7.5 Output capacitance

Refer to Figure 7.3. Output capacitors are placed both close to module (to handle the module’s output ripple) and close to the load (to handle load transients), see application note AN321 for more details. In both cases it is important with low impedance connections (to module VOUT/GND pins or to the load’s VOUT/GND pins) and the guidelines described above for the input capacitors are applied.

Note that output capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.3.

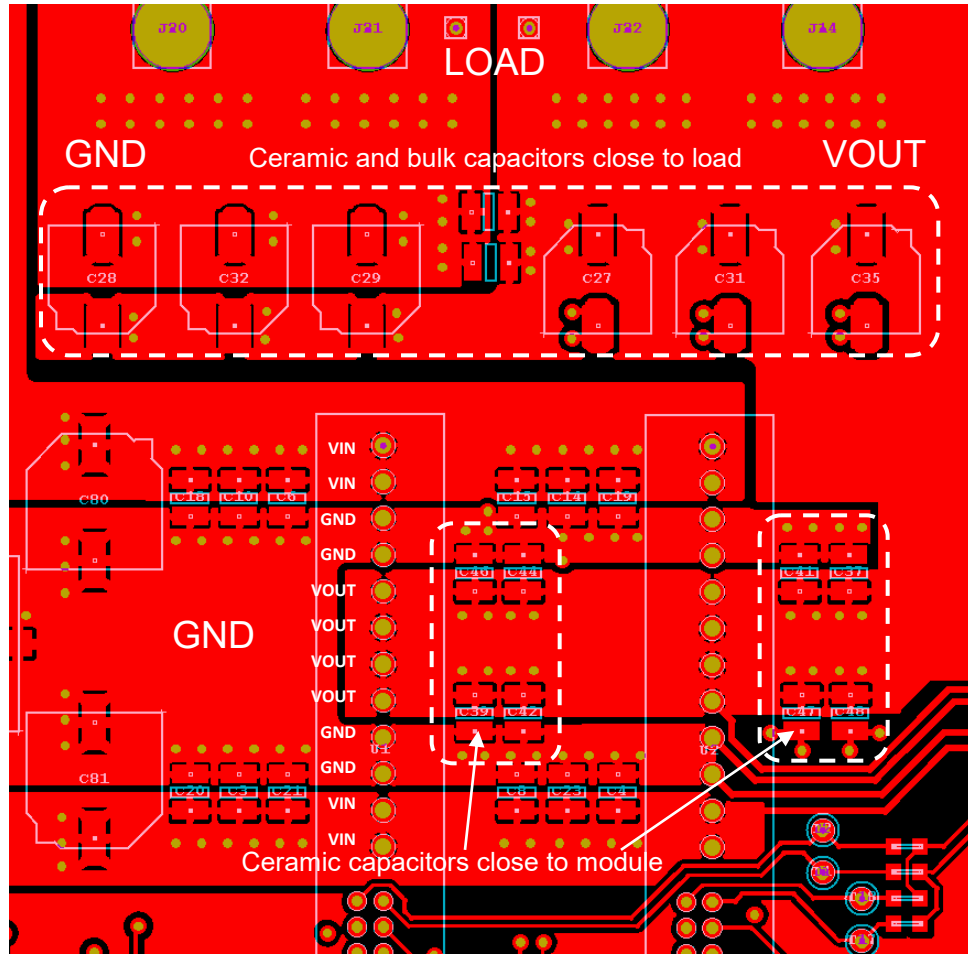


Figure 7.3. Top layer. Output capacitance in dashed areas.

Further it is important to use planes to distribute the output current to the load in order to minimize losses and the effective output impedance, providing good conditions for the module's control loop to compensate for load transient.

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7.6 Sense traces

Refer to Figure 7.4 showing the sense traces routed on Top layer and Layer 2. The traces connect at VOUT/GND points close to the load in order to provide accurate regulation. Since regulation is sensitive to disturbances on the +S/-S inputs the wires are routed as a coupled pair all the way from load to the +S/-S pins. To further provide good signal integrity a solid ground follows the traces on an adjacent layer. In this layout the sense signals are routed through jumpers and resistors, in order to provide alternatives for sensing. This is only for testing purposes however and is normally not recommended in an end application.

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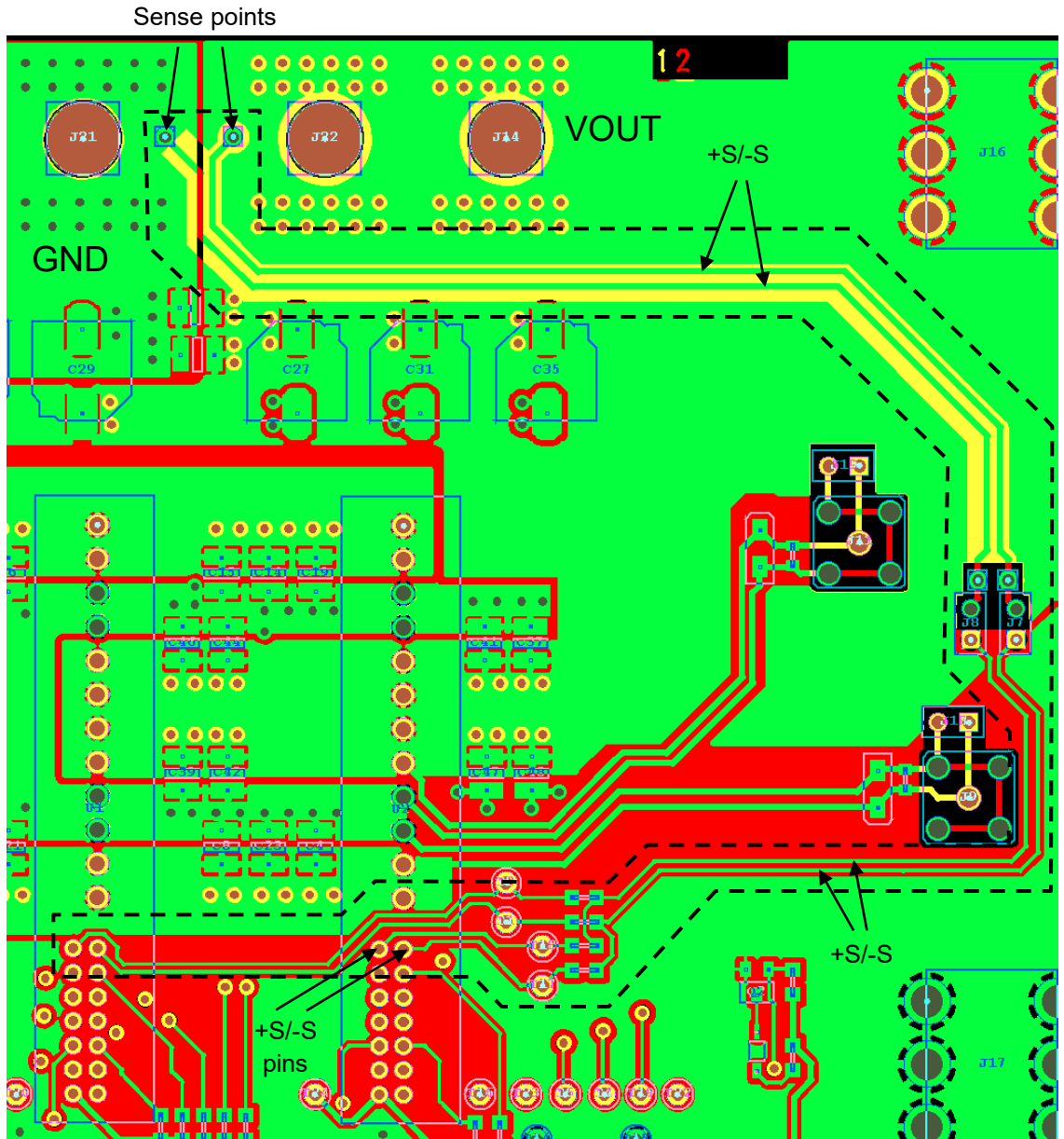


Figure 7.4. Top layer + Layer 2. Sense pair traces in dashed area.
(Yellow = Top layer, Red = Layer 2, Green = Overlap of both layers)

Both modules sense at the same points, which must be the case when the modules are operated in current sharing mode.

7.7 Pin-strap resistors

Refer to Figure 7.5 showing the routing of the pin-strap resistors circuitry. To minimize capacitive load and provide good signal integrity, the resistors are placed with short traces close to the module and with a solid ground plane on an adjacent layer.

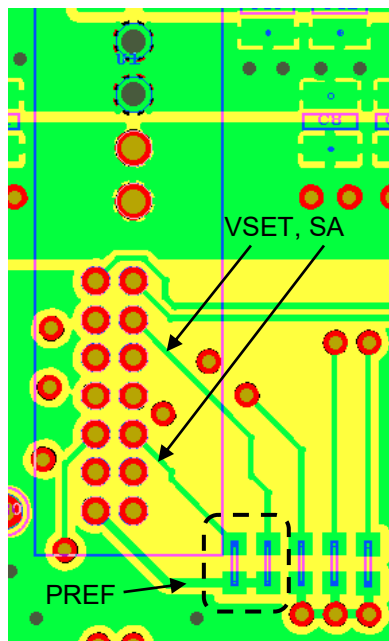


Figure 7.5. Top layer. Pin-strap resistors in dashed area.
(Red = Top layer, Yellow = Layer 2, Green = Overlap of both layers)