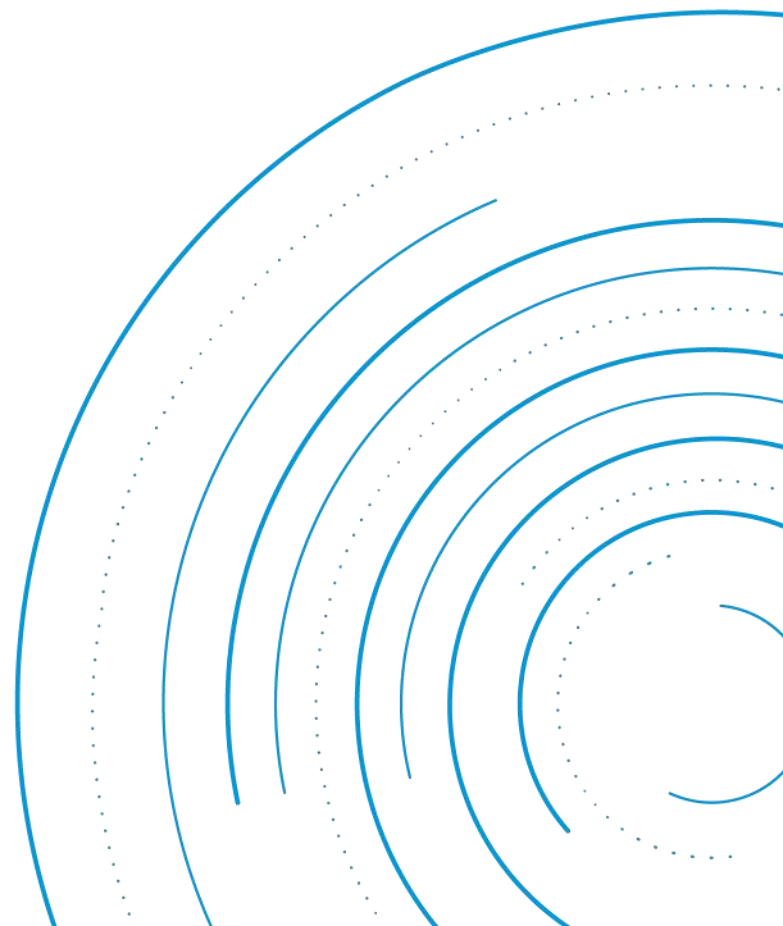


APPLICATION NOTE 321

Output filter impedance design for digital Point of Load (PoL) regulators



Abstract

The digital products can be configured, controlled and monitored through a digital serial interface using the PMBus™ power management protocol.

This application note provides information on how to design the output filter impedance of digital PoL regulators.

This application note applies to the following products:

- BMR461
- BMR462
- BMR463
- BMR464
- BMR465
- BMR466
- BMR467
- BMR469
- BMR473
- BMR474

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Component characteristics

In this application note output filter impedance design aspects and guidelines of digital Point of Load (PoL) regulators are discussed and presented.

In general, any type and model of bulk and decoupling capacitors can be used for your loop compensation and output impedance design of the PoL. However, in this application note the number of models and types has been limited to a small value by selection. Our recommendations are based on these selections. By looking into your specific vendor's datasheet you should still be able to use the method described in later sections of this application note.

Definitions

In this document we will use the following definitions:

Bulk capacitors: Decoupling capacitors which carry the majority of energy needed for the low-frequency portion of the filter.

Ceramic capacitors: Decoupling capacitors which take care of the high-frequency filtering.

Ceramic capacitors

In this application note, [Murata's ceramic capacitor](#) datasheet, tools and models will be referenced.

DC derating of capacitance value

Ceramic capacitors suffer from DC bias derating, i.e., the effective capacitance decreases with DC voltage applied to the capacitor as seen in Figure 1. In order to get a proper small signal model for the control loop design one must use the derated capacitance value, i.e., use the derated value at the output voltage operating point. It should be noted that the DC derating does not add to the component tolerance uncertainty, since the output voltage is regulated to its configured level, which can be regarded as constant.

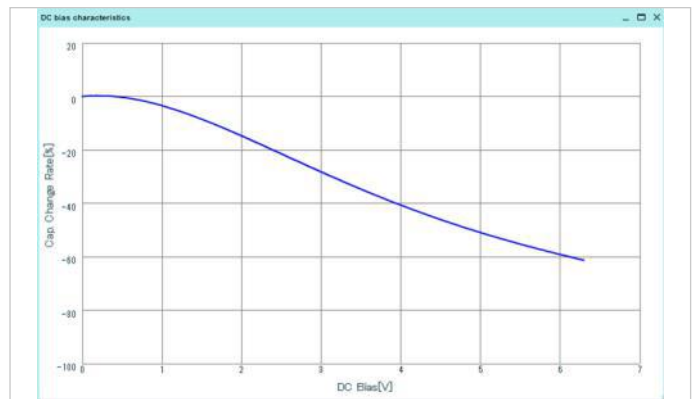


Figure 1: DC bias derating of capacitance value in ceramic capacitors

Temperature derating of capacitance value

Another uncertainty that the designer has to consider is temperature derating of the capacitance as shown in Figure 2. This derating value has to be added to the normal component tolerance.

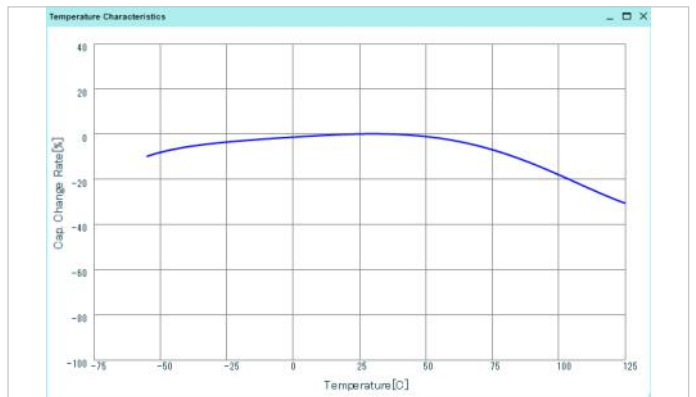


Figure 2: Temperature derating of capacitance value in ceramic

Frequency dependency of ESR value

The Equivalent Series Resistance (ESR) of a ceramic capacitor varies with frequency, often several tens of times in size. The value the designer should use in the control loop design is the value that is valid in the frequency range of the control loop bandwidth. The area to find this value is indicated in Figure 3. This parameter is identified as the Loop-ESR. As a rule of thumb, the maximum available control loop bandwidth is $f_s/10$, where f_s is the switching frequency.

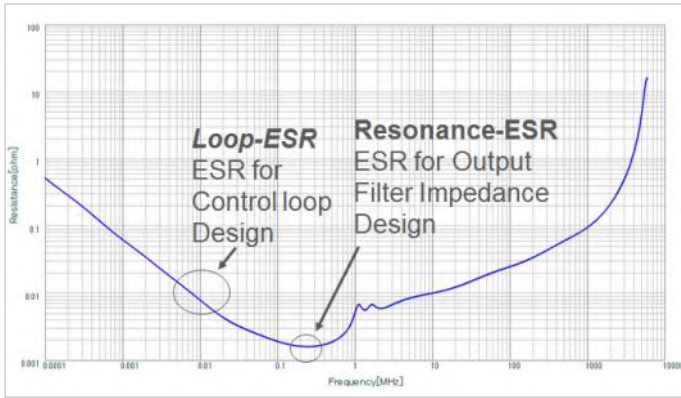


Figure 3. Frequency dependency of ceramic capacitor's ESR value from vendor TS

The ESR value that one should use in output impedance design is the ESR at the resonance frequency, i.e., the minimum value of in the curve in Figure 3 above. This parameter is identified as the Resonance-ESR

Bulk capacitors

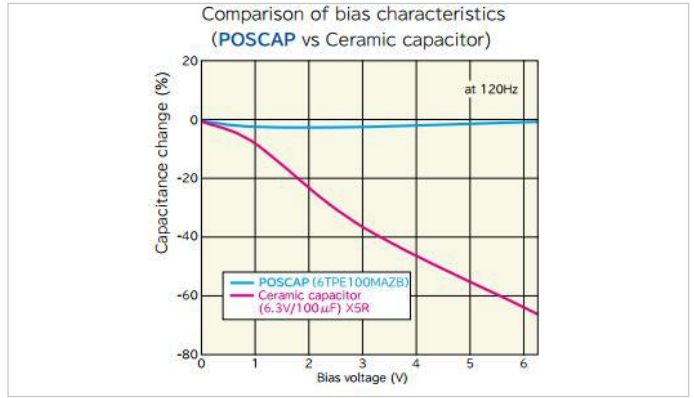
In this application note, Sanyo's electrolytic capacitor data sheet and models will be referenced.

Electrolytics are often used as bulk capacitors, i.e., the energy reservoir for the power delivery system delivering power during load transients.

The bulk capacitors suitable for decoupling of switched mode power stages should have low ESR, i.e., in the range of 5 - 50 mΩ.

DC and temperature deratings of capacitance value

OS CON and POS-CAP are two technologies that are highly suitable as bulk capacitors. Both types are very temperature stable - the capacitance change over the whole operating temperature range is less than 10%. This is significantly better than for ceramic capacitors as seen in Figure 4.



Legend:
 OS = OS-CON _____ purple
 Al = Al.-E. Cap _____ blue
 Ta = Tantalum Cap _____ green
 CR(X5P) = Cera Cap (X5P type) __red
 CR(X5U) = Cera Cap (X5U type) __pink

Figure 4. Temperature effect on capacitance value in OS-Con capacitor in comparison

In addition, neither POS-CAP nor OS-CON type capacitors suffer from DC bias derating or frequency dependency of the ESR. Hence no distinction between Loop-ESR and Resonance-ESR has to be made.

POS-CAP and OS-CON come in many different series. The POS-CAP TPF series, and the OS-CON SVPE and SVPC series are the recommended series, since low ESR is preferable. This is due to the fact that a lower ESR is more efficient than a larger capacitance when it comes to reducing load transient deviations.

Example

For a certain design the following two types of output filter solutions are compared:

Type 1: 470 μF/10mΩ

Type 2: 1500μF/20mΩ

The resulting low-to-high and high-to-low load transient responses are presented in Table 1.

Output filter type	Output voltage deviation load transient
1	105/112
2	107/116

Table 1: Output filter voltage deviation in case of low-to-high load transients

As seen, even if the capacitance value is made three times lower and the ESR is two times lower the load transient performance remains very much the same.

Ferrite beads

Ferrite beads can be used as small inductors to form pi-filters. The ferrite beads work like frequency dependent inductance and resistance. This effectively filters high frequency noise while DC current flows easily through the component, with just a few mΩ resistance. By using ferrite beads, high frequency noise from the load can be prevented to enter the PoL product and/or another load which is connected to the same PoL product .

Note: Ferrite beads will not be included in this application note.

Output filter impedance aspects

Paralleling of capacitors

When a couple of capacitors are paralleled the capacitor model's complexity does not change (as long as identical capacitors are used), i.e., the number of poles and zeros are unchanged.

The impedance, $Z(s)$, of N identical capacitors, each with capacitance value C and ESR value ESR , in parallel is shown below

$$Z(s) = 1 / \sum_{n=1}^N \frac{1}{ESR_n + \frac{1}{sC_n}} = \frac{ESR}{N} + \frac{1}{sCN} \quad (E:1)$$

The resulting capacitance is NC . The resulting ESR is ESR/N . This is exactly what is normally requested: A larger C and lower ESR.

Looking at the resulting time constant, τ_{Bank} , it turns out it is constant and independent on N . That is, it is equal to time constant of the single capacitor, as seen below.

The two equations above can be used for simplification of models and before entry of input parameters to the output filter design in [Flex Power Designer](#).

(E:2)

$$\tau_{Bank} = C_{Bank} ESR_{Bank} = NC ESR / N = C \cdot ESR$$

For example, two pieces of 50 μF /20 m Ω is equivalent to one piece of 100 μF /10 m Ω from both C and ESR perspective and a time constant perspective.

$$Z(s) = 1 / \sum_{n=1}^N \frac{1}{ESR_n + \frac{1}{sC_n}} = \frac{ESR}{N} + \frac{1}{sCN} \quad (E:3)$$

The equations above can be expanded by including the Equivalent Series Inductance, ESL. As shown below, the ESL also gets smaller by the factor of N .

Impedance of a ceramic capacitor

A capacitor has parasitic elements that vary in values with the technologies by which they are manufactured e.g., dielectric, and package.

A ceramic capacitor can be electrically modeled with lumped elements described by the parasitic elements. i.e., the ESR and ESL, and the ideal capacitor. These three elements are all in series, as illustrated in Fig 5. It shall be noted that the ESL and ESR are more dependent on package than on the capacitance value level. This implies that once you have found the capacitance value, you should select the smallest package.

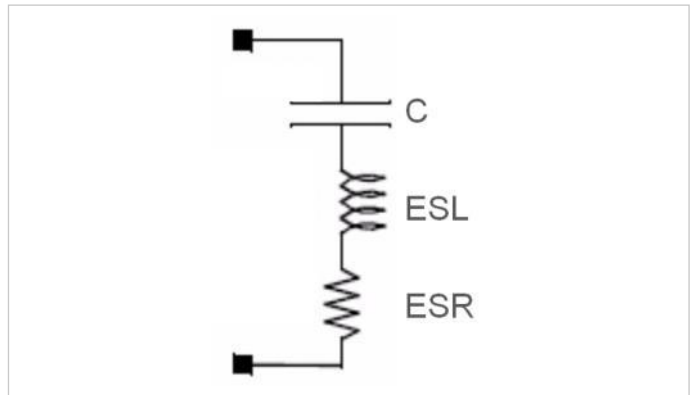


Figure 5. Electrical model of a capacitor including parasitic elements for ESR and ESL

The circuit in Figure 5 forms a series resonance circuit. At low frequencies the component impedance is dominated by the capacitor. At the resonance frequency the impedance is equal to the Resonance-ESR. Above the resonance frequency the impedance is dominated by the ESL. In Figure 6, the impedance as a function of the frequency, $Z(f)$, of a ceramic capacitor is presented.

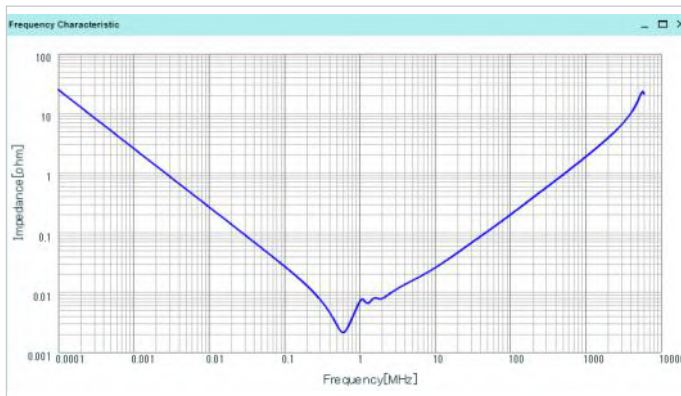


Figure 6. Impedance as function of frequency , $Z(f)$ of a ceramic capacitor

This particular capacitor works as a capacitor up to 600kHz, which is, in most cases, well beyond the control loop bandwidth. Hence, the ESL is not needed in the model when designing the control loop.

While for output impedance calculations from low frequencies (a few kHz) up to several 100s of MHz the ESL is required to be included in the model

Note: Manufacturing vendors of capacitors often provide more advanced spice models than just this 3 part model.

Control loop versus output impedance

Again, it shall be noted that two different models are needed for output filter design, one for the low frequency control loop design, and one for the high frequency impedance design.

The capacitance value for the control loop model should be the DC-derated nominal value. The ESR for the control loop model should be the Loop-ESR value valid for the frequency range around the filter's resonance frequency 10 - 30kHz range as discussed in a previous section.

The ESL is normally only used for higher frequencies during load transients and ripple simulations and impedance design. The effect of the ESL will be visible in PSpice simulations at very high frequencies.

Products on-board capacitor design considerations

The PoL itself has an onboard output capacitor, which value can be found in the product's Technical Specification, known as the internal output capacitance. This has to be accounted for when designing your decoupling capacitor bank.

In order to get a higher damping ratio that in turn allows aggressive loop compensation (this is the same as aiming for a lower Q-value of the power train), the output capacitance should be at least 2 -3 times the product's internal output capacitance.

In table 2, an example of the influence of increasing the output capacitance for a BMR463 product, with 2 pieces of 100 μ F/5m Ω ceramic output capacitors with optimized load transient configuration in each case, is shown.

No external capacitor (100 μ F)	Power train damping ratio	Load transient voltage deviation (mV)
0	0.17	385
2	0.20	209
4	0.24	173
6	0.27	133

Table 2: Capacitance influence on damping ratio and output voltage deviations

As seen, the damping ratio of the power train is almost doubled, from 0.17 to 0.27, when increasing the external capacitance from 0 to 3 times larger than the Internal Output Capacitance (this means 0 or 6 pieces of 100 μ F/5m Ω capacitors). Thanks to a higher damping, the control loop can be optimized using a more aggressive setting of the PID coefficients (The PID optimization is made by using the Flex Power Designer SW). As a result, a significant reduction of the output voltage deviation at a load transient was possible to achieve.

Output filter design of BMR product

The BMR product's output impedance must be included in the output filter impedance design. The output impedance of the BMR product is dependent on the control loop configuration. Therefore, the control loop design will be a part of the output impedance design and vice versa resulting in an iterative design process.

Output filter impedance design

As mentioned earlier, the output filter design includes two parts: control loop design and output impedance design. This section, will only focus on the output impedance design.

Ideally, the output impedance shall be flat over the whole frequency range. In practice this is not achievable. By following some design guidelines for capacitor selection however, the impedance level most often can be achieved sufficiently good over the frequency range of interest. In the following, such design guidelines are presented.

Mixing of ceramic capacitors

In many cases you would like to reduce the impedance at higher frequencies. This can be achieved by mixing different values and sizes of the ceramic capacitors over the frequency range of interest. But, then care has to be taken of anti-resonance spikes. In Figure 7 and 8, an anti-resonance spike at around 150 MHz created from paralleling of one 22nF and one 100pF ceramic capacitor is illustrated.

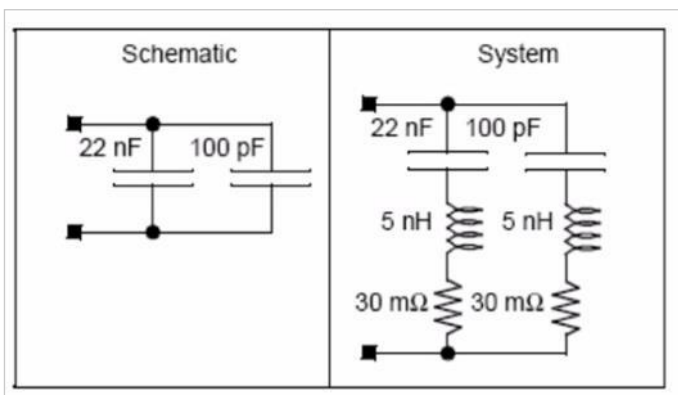


Figure 7. Illustration of anti-resonance—*influencing parasitic components*

As seen, the anti-resonance spike frequency is found close to the resonance frequency of the 100pF capacitor.

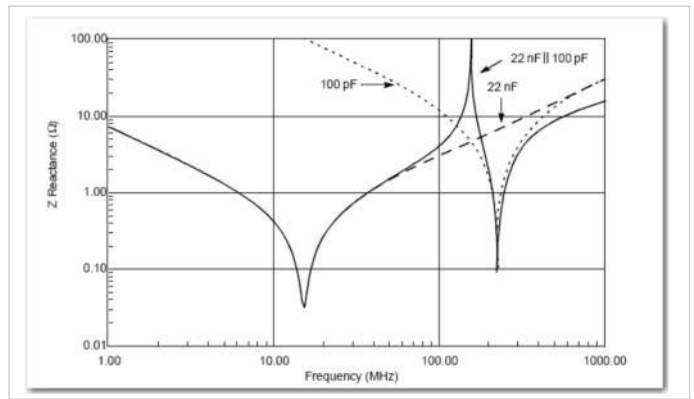


Figure 8. Illustration of anti-resonance—*influencing parasitic components*

It shall be noted that the effect of anti-resonance will increase even further with a tighter layout and usage of more efficient components. Fortunately, there exists a method to avoid or at least reduce the effect of anti-resonance when using a mix of capacitors.

Guideline for reduction of anti-resonance spikes

The most efficient way of avoiding anti-resonance spikes is to use only one type of ceramic capacitor.

In order to still keep the output impedance at lowest possible level the maximum capacitance value in a given package size should be used. If two packages offers the same capacitance value, the smallest package shall be used, since the parasitic inductance, ESL, then will be smaller.

If the impedance of the output filter is still too high, you need to use a mix of several ceramic capacitor types.

Guidelines

Then the following guidelines will help you reduce the effects of anti-resonance:

- Use only one capacitance value per decade
- Select the maximum capacitance value per package size
- Double the number of capacitors of each type between two consecutive types, going from a larger to a smaller package.

Mixing of ceramic and electrolytic capacitors

An electrolytic capacitor does not have a pronounced series resonance frequency. Therefore, its impedance is quite flat over a larger frequency range (still at low frequencies).

Due to the fact that the electrolytic typically operates at a much lower frequency than the ceramic capacitors, it has no effect on the impedance at higher frequencies. Therefore, there is no concern with mixing different types or sizes of electrolytic capacitors.

Guidelines

The recommendation is to use only one type of electrolytic capacitor. Choose the capacitor with minimum ESR value rather than a capacitor with a higher capacitance value, since this will improve the load transient performance.

Placement of ceramic and electrolytic capacitors

Placement of decoupling capacitors is in theory quite simple - place it as close as possible to the consumer load. In practice, it is not so simple and we want to share some general guidelines.

Guidelines

Below the placement of different types of capacitors, from the largest bulk capacitors to the smallest ceramic capacitor is presented.

Bulk capacitors OS-CON, POS-CAP

- Delivers power in the frequency range above the loop bandwidth
- Placement: Not so critical but as close to the load as possible

Large ceramics 1210, 100 μ F

- Low-middle frequency range
- Handle ripple current from our module, place close to Flex Power Modules product.

Large ceramics 1206, 0805 22-47 μ F

- Middle frequency
- Place within 50 mm from loads outer edge

Small ceramics 0805, 0603, 4.7-10 μ F

- Middle-High frequency
- Place within 25 mm from loads outer edge

Smallest ceramics, 0201, 0402 0.47-1 μ F

- Placement between the via pads on the opposite side of the load

Example

In Table 3, an example of an output filter design for [BMR463](#) with internal output capacitance, C_{out} equal to 200 μ F is presented

Type	C (μ F)	# of caps	Total C(μ F)
Bulk	470	2	940
1210	100	5	500
0603	10	10	100
0402	1	20	20

Table 3. Example result of BMR463 output filter design

Model of PoLs output impedance

Some ASIC/FPGA vendors' application notes and impedance calculations tools for power supply filtering require extracted output impedance parameters of the PoL. Therefore, the PoL's output impedance has to be included in the output impedance design. In this section, one method to extract the output impedance model of a PoL using the [Flex Power Designer](#) (called FPD below) is described.

Method

The procedure to extract the PoL's output impedance, and in specific, the inductance L_{POL} and resistance R_{POL} (both in series), include the following steps:

1. Enter the PoL's output filter parameter in FPD. Enter the capacitor values known at this stage (the output impedance design process is iterative, as will be seen later in this document). As a start, use the capacitors with the maximum capacitance.
2. Design/optimize the control loop parameters (PID_TAPS) using one of the FPD output filter wizards/ guides according to your design goal.
3. Open and study the output impedance plot.
4. From the output impedance plot: Take data points at two frequencies, separated as much as possible but well below the resonance peak frequency: The first one decade below the resonance peak, f_1 . The other point another decade below, f_2 .
5. Calculate L_{POL} and R_{POL} of the PoL's output, using the equations below.

The impedance at each frequency point is related as

$$\begin{aligned} f_1 : Z_1^2 &= R^2 + 4\pi^2 f_1^2 L^2 \\ f_2 : Z_2^2 &= R^2 + 4\pi^2 f_2^2 L^2 \end{aligned} \quad (E:4)$$

By identifying $L_{POL} = L$ and $R_{POL} = R$ and solving for the L and R the following equations are obtained.

$$L_{POL} = \sqrt{\frac{Z_1^2 - Z_2^2}{4\pi^2(f_1^2 - f_2^2)}} \quad (E:5)$$

$$R_{POL} = \sqrt{Z_2^2 - 4\pi^2 L_{POL}^2 f_2^2} \quad (E:6)$$

Example

The following capacitors are located between the PoL and the load:

One piece of 470 μ F/10 m Ω bulk capacitor at each side of the pi-filter inductance, five pieces of 100 mF/5 μ Ω near the POL product, ten pieces of 100 mF/5 μ Ω near the load. The filter inductance is estimated to 20 nH with total resistance of 2 m Ω .

After entry in FPD, the output filter shall look like shown in Figure 9.

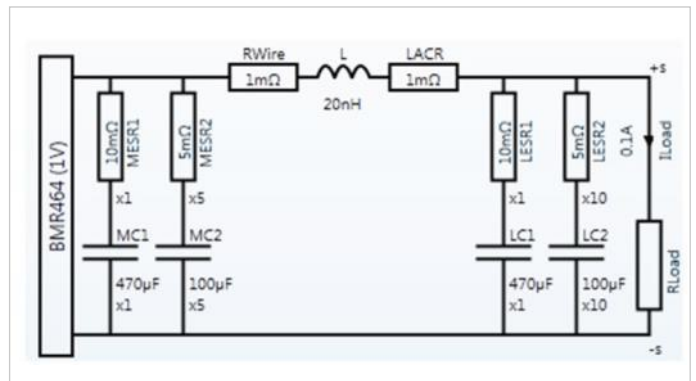


Figure 9: Example of output filter parameter values entered in Flex Power Designer

Now, design and/or optimize the PID according to your goals.

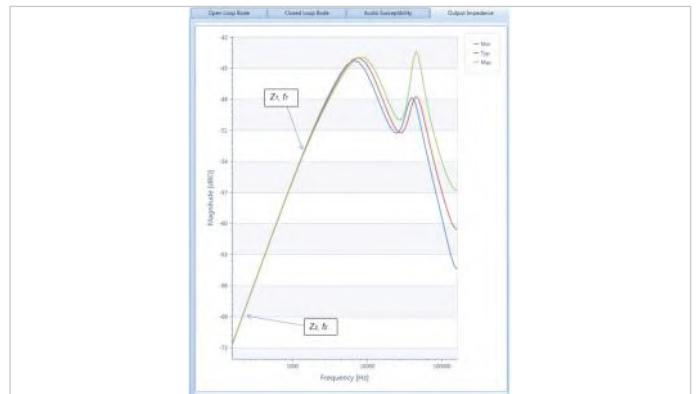


Figure 10: Example output impedance plot (FPD) illustrating data point selections made for PoL output impedance calculation

From the output impedance plot (see Figure 10): At the slope in the left part of the plot, take two data points as far as possible away from each other. First, select the (Z_1, f_1) point well below the resonance frequency and below the frequency where the Typ, Max and Min curves deviates from each other. By doing this, the output impedance extracted will be valid for component tolerances as well. The second data point, (Z_2, f_2) , is chosen approximately one decade, f_1 .

The L_{POL} and R_{POL} parameter extractions using the selected data points are shown in Figure 11 below.

$$f_1 = 1366.524 \quad Z_1 = 10^{(Z_1, dB/20)} = 10^{(-53.543/20)} \approx 2.10 m\Omega$$

$$f_2 = 196.772 \quad Z_2 = 10^{(Z_2, dB/20)} = 10^{(-69.861/20)} \approx 0.321 m\Omega$$

$$L_{POL} = \sqrt{\frac{Z_1^2 - Z_2^2}{4\pi^2(f_1^2 - f_2^2)}} \approx 0.244 \mu H \approx 0.24 \mu H \quad (E:7)$$

$$R_{POL} = \sqrt{Z_2^2 - 4\pi^2 L_{POL}^2 f_2^2} \approx 0.1 m\Omega \quad (E:8)$$

In this example, the extracted output resistance parameter of the POL, R_{POL} , is approximately 0.1 m Ω . Such a low value is normally negligible.

The extracted output inductance parameter of the POL, $L_{POL} = 0.24$ mH, is most significant and should therefore be added to the ASIC/FPGA vendor's output impedance calculation tool or to your own simulation tool.

Recommended design flow

As mentioned earlier, the output impedance design is tightly correlated with the control loop design. Therefore the design flow will include both output impedance and control loop design and in an iterative way.

It is recommended to use the ASIC/FPGA vendor's application notes and impedance calculations tools for power supply filtering. As an alternative, a spice simulator can be used. Regardless of which simulation or calculation tool is used, it will be referred to as the simulator tool in the following.

Below a recommended design flow is described. BMR462 will be used as a design example.

1. Calculate the energy reservoir needed and choose an appropriate bulk capacitance, $C_{o,ext}$, at the output of the BMR462 product based on that. The selected $C_{o,ext}$ shall be greater than the minimum recommended value in the products Technical Specification. If it is, then the default loop compensation parameters can be kept, if wanted. In this case, we select OS-CON SVPC 1200 μ F. At this stage, use your simulator tool to check that the output impedance is below requirement at low frequencies.

2. Now it is time to add ceramic capacitors of the BMR462 output. At this stage, we introduce the parameter n , which is a real integer number. First, we set $n = 1$.

3. Then, use the rule of thumb to design the ceramic capacitors. In our case, we start with n pcs of 100 μ F in 1210 package, $n \times 2$ pcs of 10 μ F in 0805 package, $n \times 22$ pcs of 1 μ F in 0603 package, and finally $n \times 23$ pcs of 0.1 μ F in 0402

4. Now, perform a new loop compensation design of the BMR462 in Flex Power Designer. From the output impedance plot, extract the low frequency output inductance. In our case, 100nH was extracted.

5. Perform a new impedance simulation using your simulator tool. If the output impedance goal over the desired frequency range is met, then you are done. If not, increase n by one, i.e. set $n = n+1$ and perform a redesign from step 3 above.

In our case, n was selected to be 3. That is, the design ended up in:

- 3 pcs of 100 μF ceramic capacitors in 1210
- 6 pcs of 10 μF ceramic capacitors in 0805
- 12 pcs of 1 μF ceramic capacitors in 0603
- 24 pcs of 0.1 μF ceramic capacitors in 0402

Note 1: If your design goals are still not met, then the bulk capacitance can be increased and/or the mix ceramic capacitor types and number can be tuned.

Note 2: Every time the number or type of capacitors is updated, the control loop should be redesigned for optimal performance and the output inductance and resistance should be re-extracted.

Validation

In this section, two output filter impedance design examples are presented. The validation has been done with Spice simulations using capacitor suppliers' simulation models available from the suppliers' web sites.

Validation example 1 - rule of thumb

The selected product is BMR462. The design requirement is maximum 20m Ω up to 100 MHz. The design results following Recommended Design Flow in previous section is presented in the table below

Type	Value (μF)	Number of capacitors	Total capacitances (μF)	Total capacitances @ 1V (μF)
Bulk	1200	1	1200	1200
1210	100	3	300	285
0805	10	6	60	57
0603	1	12	12	11.4
0402	0.1	24	2.4	2.28

Table 4. Example 1—rule of thumb BMR462 output filter impedance

The validation was performed in a PSpice simulator. The result is shown in figure 11.

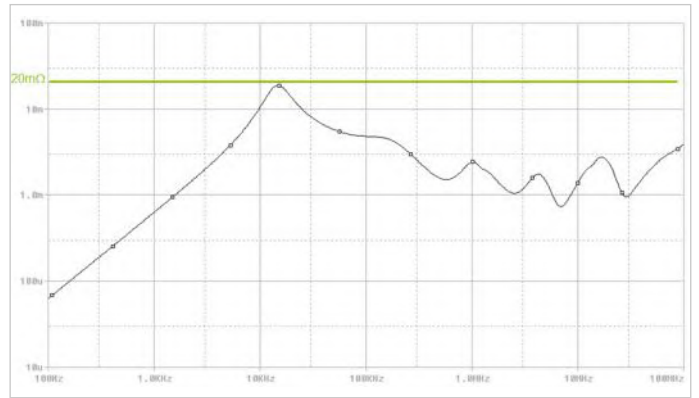


Figure 11: Example 1 -Rule of Thumb design of BMR 462 output filter impedance - Result in PSpice simulation using vendors' SPICE models.

Validation Example 2 - design for flat output impedance

The selected product is the same as in Example 1, i.e. BMR462. The design results following rule of thumb in previous section is however not flat enough, or in other words, the output impedance is unnecessary low in the 1 - 10 MHz frequency range. Goal target is to keep the impedance just below 10m Ω in the 1 - 10 MHz frequency range. This will give us some margin to the 20 m Ω requirement. By reduction of the number of ceramic capacitors this should be possible to achieve.

By manual work, the optimized result in table below

Type	Value (μF)	Number of capacitors	Total capacitances (μF)	Total capacitances @ 1V (μF)
Bulk	1200	1	1200	1200
1210	100	1	100	95
0805	10	5	50	47.5
0603	1	10	10	9.5
0402	0.1	11	11	1.1

Table 5. Example 2 - result of BMR462 output filter design optimization for a flat impedance below 20m Ω in the 100 Hz - 100 MHz frequency range

The validation was performed in a PSpice simulator. The resulting output impedance is shown in Figure 12.

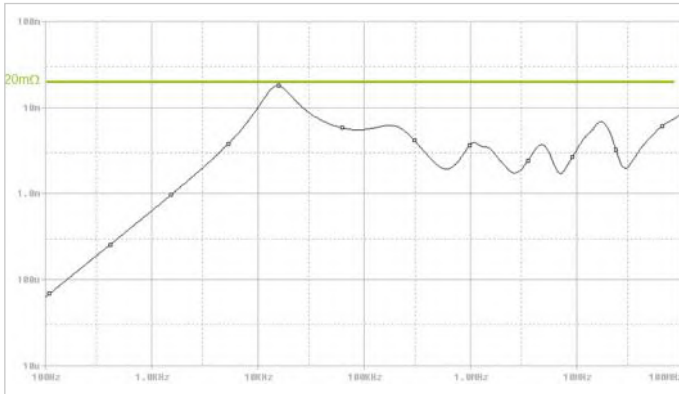


Figure 12: Example 2 - Optimized output impedance design of BMR462 output filter - Result in PSpice simulation using vendor's SPICE models.

As seen, the impedance is still below 20 mΩ in the whole frequency range, but the impedance level is increased somewhat in the 1 -10 MHz region as requested. Hence the design goal is met, achieved with a smaller amount of ceramic capacitors.



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